



# AD7846—SPECIFICATIONS<sup>1</sup>

( $V_{DD} = +14.25\text{ V to }+15.75\text{ V}$ ;  $V_{SS} = -14.25\text{ V to }-15.75\text{ V}$ ;  $V_{CC} = +4.75\text{ V to }+5.25\text{ V}$ .  
 $V_{OUT}$  loaded with  $2\text{ k}\Omega$ ,  $1000\text{ pF}$  to  $0\text{ V}$ ;  $V_{REF+} = +5\text{ V}$ ;  $R_{IN}$  connected to  $0\text{ V}$ . All  
specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.)

Parameter	J, A Versions	K, B Versions	Unit	Test Conditions/Comments
RESOLUTION	16	16	Bits	
UNIPOLAR OUTPUT				$V_{REF-} = 0\text{ V}$ , $V_{OUT} = 0\text{ V to }+10\text{ V}$ 1 LSB = $153\text{ }\mu\text{V}$
Relative Accuracy @ $+25^{\circ}\text{C}$	$\pm 12$	$\pm 4$	LSB typ	All Grades Guaranteed Monotonic $V_{OUT}$ Load = $10\text{ M}\Omega$
$T_{MIN}$ to $T_{MAX}$	$\pm 16$	$\pm 8$	LSB max	
Differential Nonlinearity Error	$\pm 1$	$\pm 0.5$	LSB max	
Gain Error @ $+25^{\circ}\text{C}$	$\pm 12$	$\pm 6$	LSB typ	
$T_{MIN}$ to $T_{MAX}$	$\pm 16$	$\pm 16$	LSB max	
Offset Error @ $+25^{\circ}\text{C}$	$\pm 12$	$\pm 6$	LSB typ	
$T_{MIN}$ to $T_{MAX}$	$\pm 16$	$\pm 16$	LSB max	
Gain $\text{TC}^2$	$\pm 1$	$\pm 1$	ppm $\text{FSR}/^{\circ}\text{C}$ typ	
Offset $\text{TC}^2$	$\pm 1$	$\pm 1$	ppm $\text{FSR}/^{\circ}\text{C}$ typ	
BIPOLAR OUTPUT				$V_{REF-} = -5\text{ V}$ , $V_{OUT} = -10\text{ V to }+10\text{ V}$ 1 LSB = $305\text{ }\mu\text{V}$
Relative Accuracy @ $+25^{\circ}\text{C}$	$\pm 6$	$\pm 2$	LSB typ	All Grades Guaranteed Monotonic $V_{OUT}$ Load = $10\text{ M}\Omega$
$T_{MIN}$ to $T_{MAX}$	$\pm 8$	$\pm 4$	LSB max	
Differential Nonlinearity Error	$\pm 1$	$\pm 0.5$	LSB max	
Gain Error @ $+25^{\circ}\text{C}$	$\pm 6$	$\pm 4$	LSB typ	
$T_{MIN}$ to $T_{MAX}$	$\pm 16$	$\pm 16$	LSB max	
Offset Error @ $+25^{\circ}\text{C}$	$\pm 6$	$\pm 4$	LSB typ	
$T_{MIN}$ to $T_{MAX}$	$\pm 16$	$\pm 12$	LSB max	
Bipolar Zero Error @ $+25^{\circ}\text{C}$	$\pm 6$	$\pm 4$	LSB typ	$V_{OUT}$ Load = $10\text{ M}\Omega$
$T_{MIN}$ to $T_{MAX}$	$\pm 12$	$\pm 8$	LSB max	
Gain $\text{TC}^2$	$\pm 1$	$\pm 1$	ppm $\text{FSR}/^{\circ}\text{C}$ typ	
Offset $\text{TC}^2$	$\pm 1$	$\pm 1$	ppm $\text{FSR}/^{\circ}\text{C}$ typ	
Bipolar Zero $\text{TC}^2$	$\pm 1$	$\pm 1$	ppm $\text{FSR}/^{\circ}\text{C}$ typ	
REFERENCE INPUT				
Input Resistance	20 40	20 40	k $\Omega$ min k $\Omega$ max	Resistance from $V_{REF+}$ to $V_{REF-}$ Typically $30\text{ k}\Omega$
$V_{REF+}$ Range	$V_{SS} + 6$ to $V_{DD} - 6$	$V_{SS} + 6$ to $V_{DD} - 6$	Volts	
$V_{REF-}$ Range	$V_{SS} + 6$ to $V_{DD} - 6$	$V_{SS} + 6$ to $V_{DD} - 6$	Volts	
OUTPUT CHARACTERISTICS				
Output Voltage Swing	$V_{SS} + 4$ to $V_{DD} - 3$	$V_{SS} + 4$ to $V_{DD} - 3$	V max	To $0\text{ V}$ To $0\text{ V}$ To $0\text{ V}$ or Any Power Supply
Resistive Load	2	2	k $\Omega$ min	
Capacitive Load	1000	1000	pF max	
Output Resistance	0.3	0.3	$\Omega$ typ	
Short Circuit Current	$\pm 25$	$\pm 25$	mA typ	
DIGITAL INPUTS				
$V_{IH}$ (Input High Voltage)	2.4	2.4	V min	
$V_{IL}$ (Input Low Voltage)	0.8	0.8	V max	
$I_{IN}$ (Input Current)	$\pm 10$	$\pm 10$	$\mu\text{A}$ max	
$C_{IN}$ (Input Capacitance) <sup>2</sup>	10	10	pF max	
DIGITAL OUTPUTS				
$V_{OL}$ (Output Low Voltage)	0.4	0.4	Volts max	$I_{SINK} = 1.6\text{ mA}$ $I_{SOURCE} = 400\text{ }\mu\text{A}$ DB0–DB15 = $0$ to $V_{CC}$
$V_{OH}$ (Output High Voltage)	4.0	4.0	Volts min	
Floating State Leakage Current	$\pm 10$	$\pm 10$	$\mu\text{A}$ max	
Floating State Output Capacitance <sup>2</sup>	10	10	pF max	
POWER REQUIREMENTS <sup>3</sup>				
$V_{DD}$	$+11.4/+15.75$	$+11.4/+15.75$	V min/V max	$V_{OUT}$ Unloaded $V_{OUT}$ Unloaded
$V_{SS}$	$-11.4/-15.75$	$-11.4/-15.75$	V min/V max	
$V_{CC}$	$+4.75/+5.25$	$+4.75/+5.25$	V min/V max	
$I_{DD}$	5	5	mA max	
$I_{SS}$	5	5	mA max	
$I_{CC}$	1	1	mA max	
Power Supply Sensitivity <sup>4</sup>	1.5	1.5	LSB/V max	
Power Dissipation	100	100	mW typ	$V_{OUT}$ Unloaded

## NOTES

<sup>1</sup>Temperature ranges as follows: J, K Versions:  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ; A, B Versions:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

<sup>2</sup>Guaranteed by design and characterization, not production tested.

<sup>3</sup>The AD7846 is functional with power supplies of  $\pm 12\text{ V}$ . See Typical Performance Curves.

<sup>4</sup>Sensitivity of Gain Error, Offset Error and Bipolar Zero Error to  $V_{DD}$ ,  $V_{SS}$  variations.

Specifications subject to change without notice.

## AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance and are not subject to test. ( $V_{REF+} = +5\text{ V}$ ;  $V_{DD} = +14.25\text{ V}$  to  $+15.75\text{ V}$ ;  $V_{SS} = -14.25\text{ V}$  to  $-15.75\text{ V}$ ;  $V_{CC} = +4.75\text{ V}$  to  $+5.25\text{ V}$ ;  $R_{IN}$  connected to  $0\text{ V}$ .)

Parameter	Limit at $T_{MIN}$ to $T_{MAX}$ (All Versions)	Unit	Test Conditions/Comments
Output Settling Time <sup>1</sup>	6	$\mu\text{s max}$	To 0.006% FSR. $V_{OUT}$ loaded. $V_{REF-} = 0\text{ V}$ . Typically $3.5\text{ }\mu\text{s}$ .
Slew Rate	9	$\mu\text{s max}$	To 0.003% FSR. $V_{OUT}$ loaded. $V_{REF-} = -5\text{ V}$ . Typically $6.5\text{ }\mu\text{s}$ .
Digital-to-Analog Glitch Impulse	7	$\text{V}/\mu\text{s typ}$	
AC Feedthrough	70	$\text{nV-secs typ}$	DAC alternately loaded with 10 . . . 0000 and 01 . . . 1111. $V_{OUT}$ unloaded.
Digital Feedthrough	0.5	$\text{mV pk-pk typ}$	$V_{REF-} = 0\text{ V}$ , $V_{REF+} = 1\text{ V rms}$ , 10 kHz sine wave. DAC loaded with all 0s.
Output Noise Voltage Density 1 kHz–100 kHz	10	$\text{nV-secs typ}$	DAC alternately loaded with all 1s and all 0s. $\overline{\text{CS}}$ High.
	50	$\text{nV}/\sqrt{\text{Hz typ}}$	Measured at $V_{OUT}$ . DAC loaded with 0111011 . . . 11. $V_{REF+} = V_{REF-} = 0\text{ V}$ .

## NOTES

<sup>1</sup> $\overline{\text{LDAC}} = 0$ . Settling time does not include deglitching time of  $2.5\text{ }\mu\text{s}$  (typ).

Specifications subject to change without notice.

## TIMING CHARACTERISTICS

( $V_{DD} = +14.25\text{ V}$  to  $+15.75\text{ V}$ ;  $V_{SS} = -14.25\text{ V}$  to  $-15.75\text{ V}$ ;  $V_{CC} = +4.75\text{ V}$  to  $+5.25\text{ V}$ )

Parameter	Limit at $T_{MIN}$ to $T_{MAX}$ (All Versions)	Unit	Test Conditions/Comments
$t_1$	0	ns min	$\overline{\text{R/W}}$ to $\overline{\text{CS}}$ Setup Time
$t_2$	60	ns min	$\overline{\text{CS}}$ Pulsewidth (Write Cycle)
$t_3$	0	ns min	$\overline{\text{R/W}}$ to $\overline{\text{CS}}$ Hold Time
$t_4$	60	ns min	Data Setup Time
$t_5$	0	ns min	Data Hold Time
$t_6$	120	ns max	Data Access Time
$t_7$	10	ns min	Bus Relinquish Time
	60	ns max	
$t_8$	0	ns min	$\overline{\text{CLR}}$ Setup Time
$t_9$	70	ns min	$\overline{\text{CLR}}$ Pulsewidth
$t_{10}$	0	ns min	$\overline{\text{CLR}}$ Hold Time
$t_{11}$	70	ns min	$\overline{\text{LDAC}}$ Pulsewidth
$t_{12}$	130	ns min	$\overline{\text{CS}}$ Pulsewidth (Read Cycle)

## NOTES

<sup>1</sup>Timing specifications are sample tested at  $+25^\circ\text{C}$  to ensure compliance. All input control signals are specified with  $t_R = t_F = 5\text{ ns}$  (10% to 90% of  $+5\text{ V}$ ) and timed from a voltage level of  $1.6\text{ V}$ .

<sup>2</sup> $t_6$  is measured with the load circuits of Figure 1 and defined as the time required for an output to cross  $0.8\text{ V}$  or  $2.4\text{ V}$ .

<sup>3</sup> $t_7$  is defined as the time required for an output to change  $0.5\text{ V}$  when loaded with the circuits of Figure 2.

Specifications subject to change without notice.

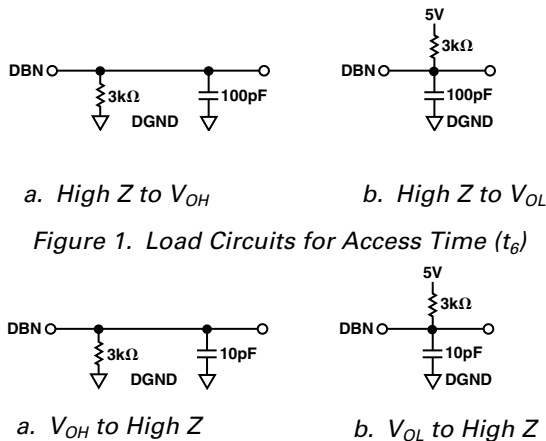


Figure 2. Load Circuits for Bus Relinquish Time ( $t_7$ )

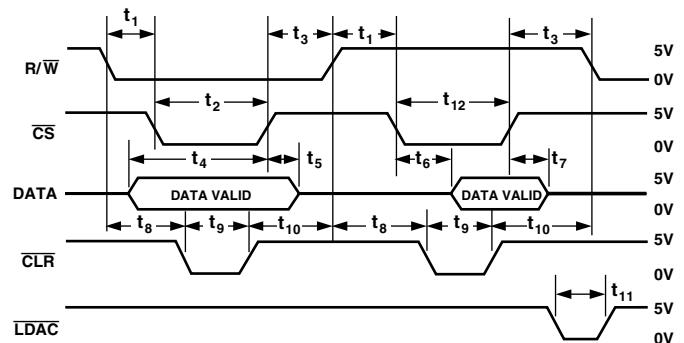


Figure 3. Timing Diagram

# AD7846

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

$V_{DD}$ to DGND	−0.4 V to +17 V
$V_{CC}$ to DGND	−0.4 V, $V_{DD} + 0.4$ V or +7 V (Whichever Is Lower)
$V_{SS}$ to DGND	+0.4 V to −17 V
$V_{REF+}$ to DGND	$V_{DD} + 0.4$ V, $V_{SS} - 0.4$ V
$V_{REF-}$ to DGND	$V_{DD} + 0.4$ V, $V_{SS} - 0.4$ V
$V_{OUT}$ to DGND <sup>2</sup>	$V_{DD} + 0.4$ V, $V_{SS} - 0.4$ V or $\pm 10$ V (Whichever Is Lower)
$R_{IN}$ to DGND	$V_{DD} + 0.4$ V, $V_{SS} - 0.4$ V
Digital Input Voltage to DGND	−0.4 V to $V_{CC} + 0.4$ V
Digital Output Voltage to DGND	−0.4 V to $V_{CC} + 0.4$ V
Power Dissipation (Any Package)	
To +75°C	1000 mW
Derates above +75°C	10 mW/°C
Operating Temperature Range	
J, K Versions	0°C to +70°C
A, B Versions	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering)	+300°C

## NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

<sup>2</sup> $V_{OUT}$  may be shorted to DGND,  $V_{DD}$ ,  $V_{SS}$ ,  $V_{CC}$  provided that the power dissipation of the package is not exceeded.

## ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Package Description	Package Options
AD7846JN	0°C to +70°C	$\pm 16$ LSB	Plastic DIP	N-28A
AD7846KN	0°C to +70°C	$\pm 8$ LSB	Plastic DIP	N-28A
AD7846JP	0°C to +70°C	$\pm 16$ LSB	Plastic Leaded Chip Carrier (PLCC)	P-28A
AD7846KP	0°C to +70°C	$\pm 8$ LSB	Plastic Leaded Chip Carrier (PLCC)	P-28A
AD7846AP	−40°C to +85°C	$\pm 16$ LSB	Plastic Leaded Chip Carrier (PLCC)	P-28A
AD7846AQ	−40°C to +85°C	$\pm 16$ LSB	Ceramic DIP	Q-28
AD7846BP	−40°C to +85°C	$\pm 8$ LSB	Plastic Leaded Chip Carrier (PLCC)	P-28A

## CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



## TERMINOLOGY

### LEAST SIGNIFICANT BIT

This is the analog weighting of 1 bit of the digital word in a DAC. For the AD7846, 1 LSB =  $(V_{REF+} - V_{REF-})/2^{16}$ .

### Relative Accuracy

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for both endpoints (i.e., offset and gain errors are adjusted out) and is normally expressed in least significant bits or as a percentage of full-scale range.

### Differential Nonlinearity

Differential nonlinearity is the difference between the measured change and the ideal change between any two adjacent codes. A specified differential nonlinearity of  $\pm 1$  LSB over the operating temperature range ensures monotonicity.

### Gain Error

Gain error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been adjusted out. Gain error is adjustable to zero with an external potentiometer.

### Offset Error

This is the error present at the device output with all 0s loaded in the DAC. It is due to op amp input offset voltage and bias current and the DAC leakage current.

### Bipolar Zero Error

When the AD7846 is connected for bipolar output and 10 . . . 000 is loaded to the DAC, the deviation of the analog output from the ideal midscale of 0 V is called the bipolar zero error.

### Digital-to-Analog Glitch Impulse

This is the amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or a voltage.

### Multiplying Feedthrough Error

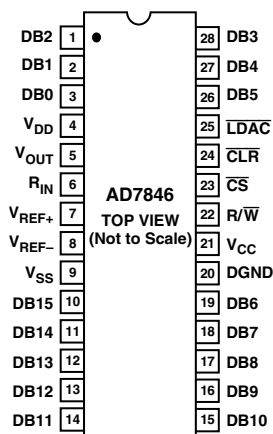
This is an ac error due to capacitive feedthrough from either of the  $V_{REF}$  terminals to  $V_{OUT}$  when the DAC is loaded with all 0s.

### Digital Feedthrough

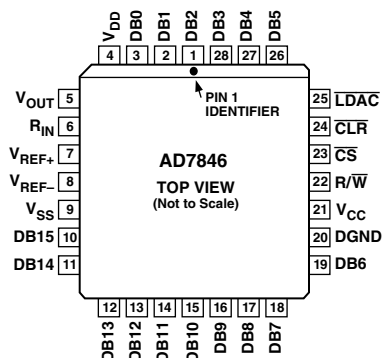
When the DAC is not selected (i.e.,  $\overline{CS}$  is held high), high frequency logic activity on the digital inputs is capacitively coupled through the device to show up as noise on the  $V_{OUT}$  pin. This noise is digital feedthrough.

## PIN CONFIGURATIONS

## DIP



## PLCC



## PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1–3	DB2–DB0	Data I/O pins. DB0 is LSB.
4	$V_{DD}$	Positive supply for analog circuitry. This is +15 V nominal.
5	$V_{OUT}$	DAC output voltage pin.
6	$R_{IN}$	Input to summing resistor of DAC output amplifier. This is used to select output voltage ranges. See Table I.
7	$V_{REF+}$	$V_{REF+}$ Input. The DAC is specified for $V_{REF+} = +5$ V.
8	$V_{REF-}$	$V_{REF-}$ Input. For unipolar operation connect $V_{REF-}$ to 0 V and for bipolar operation connect it to $-5$ V. The device is specified for both conditions.
9	$V_{SS}$	Negative supply for the analog circuitry. This is $-15$ V nominal.
10–19	DB15–DB6	Data I/O pins. DB15 is MSB.
20	DGND	Ground pin for digital circuitry.
21	$V_{CC}$	Positive supply for digital circuitry. This is +5 V nominal.
22	$R/\overline{W}$	$R/\overline{W}$ input. This can be used to load data to the DAC or to read back the DAC latch contents.
23	$\overline{CS}$	Chip select input. This selects the device.
24	$\overline{CLR}$	Clear input. The DAC can be cleared to 000 . . . 000 or 100 . . . 000. See Table II.
25	$\overline{LDAC}$	Asynchronous load input to DAC.
26–28	DB5–DB3	Data I/O pins.

Table I. Output Voltage Ranges

Output Range	$V_{REF+}$	$V_{REF-}$	$R_{IN}$
0 V to +5 V	+5 V	0 V	$V_{OUT}$
0 V to +10 V	+5 V	0 V	0 V
+5 V to $-5$ V	+5 V	$-5$ V	$V_{OUT}$
+5 V to $-5$ V	+5 V	0 V	+5 V
+10 V to $-10$ V	+5 V	$-5$ V	0 V

# AD7846—Typical Performance Curves

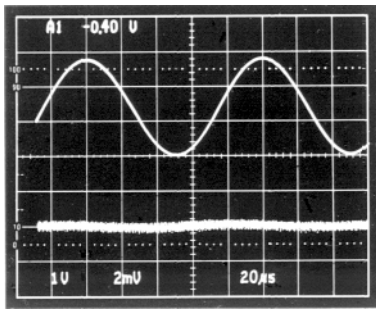


Figure 4. AC Feedthrough.  $V_{REF+} = 1 \text{ V rms}$ , 10 kHz Sine Wave

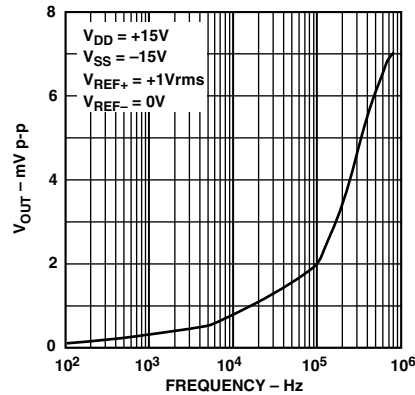


Figure 5. AC Feedthrough vs. Frequency

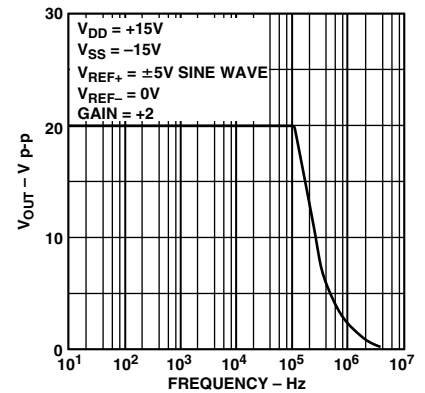


Figure 6. Large Signal Frequency Response

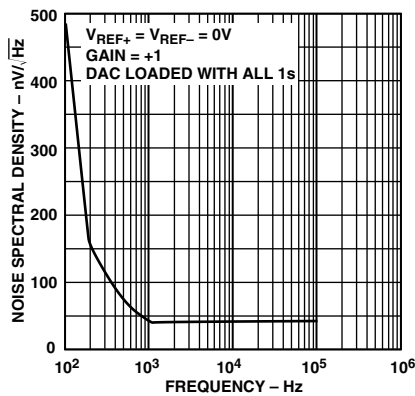


Figure 7. Noise Spectral Density

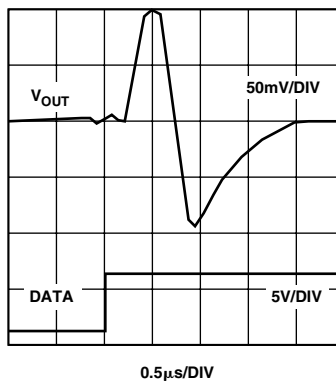


Figure 8. Digital-to-Analog Glitch Impulse Without Internal Deglitcher (10...000 to 011...111 Transition)

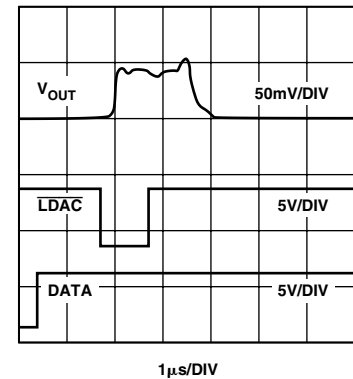


Figure 9. Digital-to-Analog Glitch Impulse With Internal Deglitcher (10...000 to 011...111 Transition)

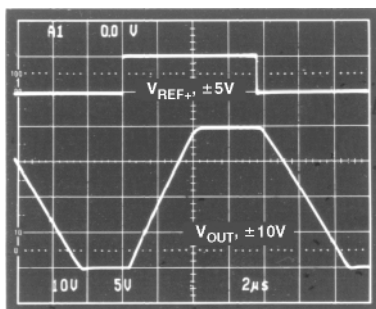


Figure 10. Pulse Response (Large Signal)

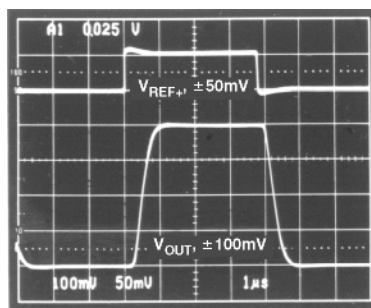


Figure 11. Pulse Response (Small Signal)

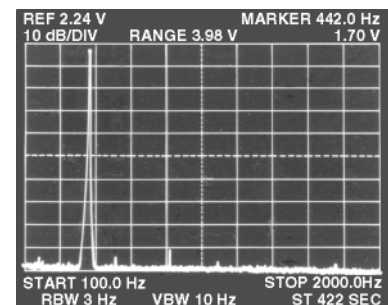
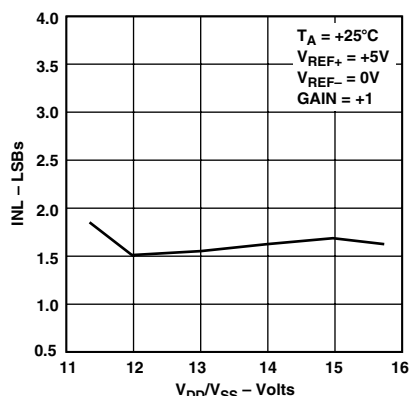
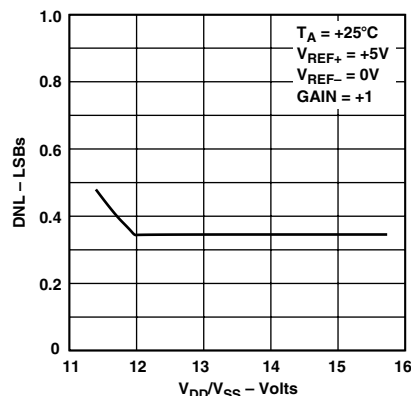


Figure 12. Spectral Response of Digitally Constructed Sine Wave

Figure 13. Typical Linearity vs.  $V_{DD}/V_{SS}$ Figure 14. Typical Monotonicity vs.  $V_{DD}/V_{SS}$ 

## CIRCUIT DESCRIPTION

### Digital Section

Figure 15 shows the digital control logic and on-chip data latches in the AD7846. Table II is the associated truth table. The D/A converter has two latches that are controlled by four signals:  $\overline{CS}$ ,  $R/\overline{W}$ ,  $\overline{LDAC}$  and  $\overline{CLR}$ . The input latch is connected to the data bus (DB15–DB0). A word is written to the input latch by bringing  $\overline{CS}$  low and  $R/\overline{W}$  low. The contents of the input latch may be read back by bringing  $\overline{CS}$  low and  $R/\overline{W}$  high. This feature is called “readback” and is used in system diagnostic and calibration routines.

Data is transferred from the input latch to the DAC latch with the  $\overline{LDAC}$  strobe. The equivalent analog value of the DAC latch contents appears at the DAC output. The  $\overline{CLR}$  pin resets the DAC latch contents to 000 . . . 000 or 100 . . . 000, depending on the state of  $R/\overline{W}$ . Writing a  $\overline{CLR}$  loads 000 . . . 000 and reading a  $\overline{CLR}$  loads 100 . . . 000. To reset a DAC to 0 V in a unipolar system the user should exercise  $\overline{CLR}$  while  $R/\overline{W}$  is low; to reset to 0 V in a bipolar system exercise the  $\overline{CLR}$  while  $R/\overline{W}$  is high.

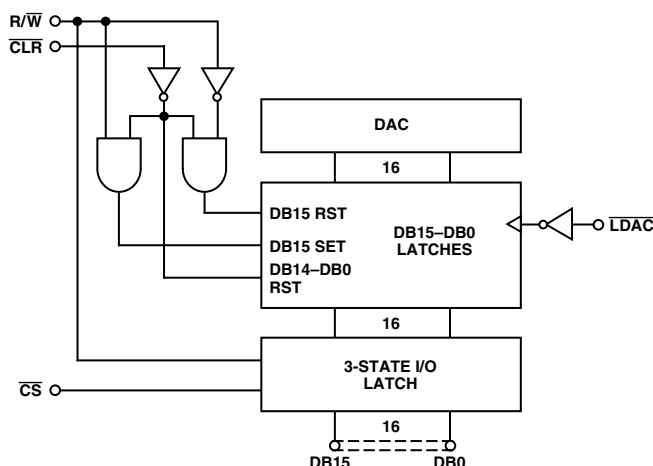


Figure 15. Input Control Logic

Table II. Control Logic Truth Table

$\overline{CS}$	$R/\overline{W}$	$\overline{LDAC}$	$\overline{CLR}$	Function
1	X	X	X	3-State DAC I/O Latch in High-Z State
0	0	X	X	DAC I/O Latch Loaded with DB15–DB0
0	1	X	X	Contents of DAC I/O Latch Available on DB15–DB0
X	X	0	1	Contents of DAC I/O Latch Transferred to DAC Latch
X	0	X	0	DAC Latch Loaded with 000 . . . 000
X	1	X	0	DAC Latch Loaded with 100 . . . 000

### D/A Conversion

Figure 16 shows the D/A section of the AD7846. There are three DACs, each of which have their own buffer amplifiers. DAC1 and DAC2 are 4-bit DACs. They share a 16-resistor string but have their own analog multiplexers. The voltage reference is applied to the resistor string. DAC3 is a 12-bit voltage mode DAC with its own output stage.

The 4 MSBs of the 16-bit digital code drive DAC1 and DAC2 while the 12 LSBs control DAC3. Using DAC1 and DAC2, the MSBs select a pair of adjacent nodes on the resistor string and present that voltage to the positive and negative inputs of DAC3. This DAC interpolates between these two voltages to produce the analog output voltage.

To prevent nonmonotonicity in the DAC due to amplifier offset voltages, DAC1 and DAC2 “leap-frog” along the resistor string. For example, when switching from Segment 1 to Segment 2, DAC1 switches from the bottom of Segment 1 to the top of Segment 2 while DAC2 stays connected to the top of Segment 1. The code driving DAC3 is automatically complemented to compensate for the inversion of its inputs. This means that any linearity effects due to amplifier offset voltages remain unchanged when switching from one segment to the next and 16-bit monotonicity is ensured if DAC3 is monotonic. So, 12-bit resistor matching in DAC3 guarantees overall 16-bit monotonicity. This is much more achievable than the 16-bit matching which a conventional R-2R structure would have needed.

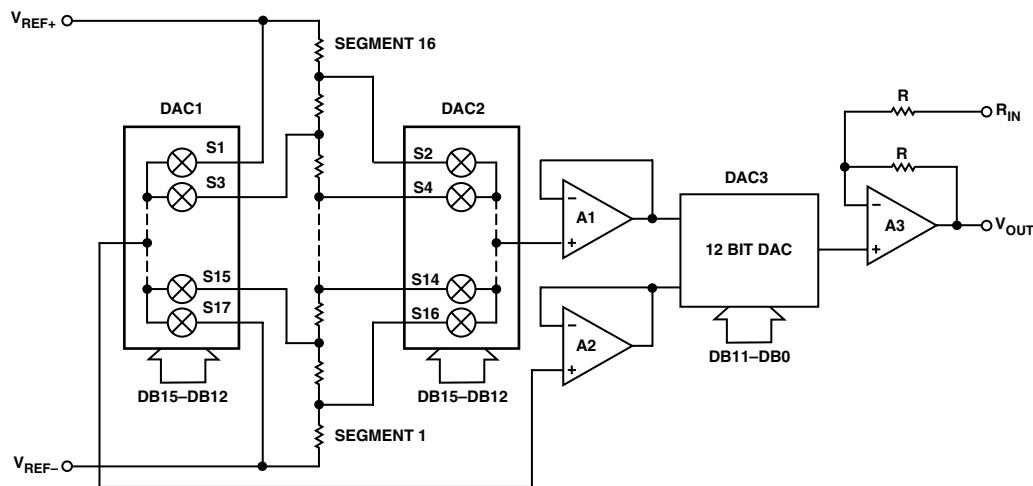


Figure 16. D/A Conversion

Output Stage

The output stage of the AD7846 is shown in Figure 17. It is capable of driving a 2 kΩ/1000 pF load. It also has a resistor feedback network which allows the user to configure it for gains of one or two. Table I shows the different output ranges that are possible.

An additional feature is that the output buffer is configured as a track-and-hold amplifier. Although normally tracking its input, this amplifier is placed in a hold mode for approximately 2.5 μs after the leading edge of LDAC. This short state keeps the DAC output at its previous voltage while the AD7846 is internally changing to its new value. So, any glitches that occur in the transition are not seen at the output. In systems where the LDAC is tied permanently low, the deglitching will not be in operation. Figures 8 and 9 show the outputs of the AD7846 without and with the deglitcher.

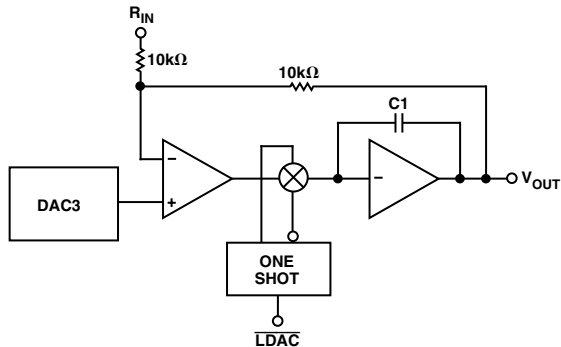


Figure 17. Output Stage

UNIPOLAR BINARY OPERATION

Figure 18 shows the AD7846 in the unipolar binary circuit configuration. The DAC is driven by the AD586, +5 V reference. Since RIN is tied to 0 V, the output amplifier has a gain of 2 and the output range is 0 V to +10 V. If a 0 V to +5 V range is required, RIN should be tied to VOUT, configuring the output stage for a gain of 1. Table III gives the code table for the circuit of Figure 18.

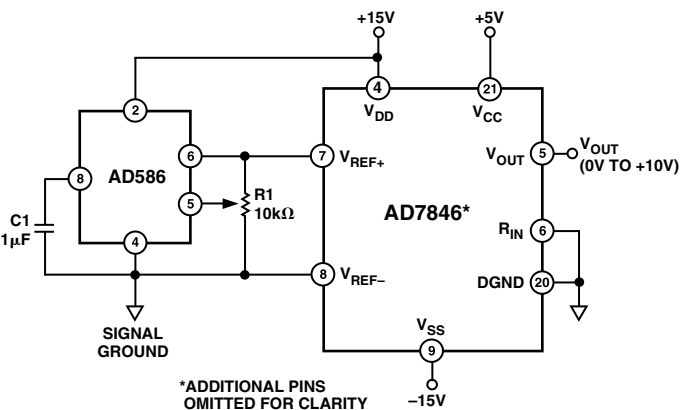


Figure 18. Unipolar Binary Operation

Table III. Code Table for Figure 18

Binary Number in DAC Latch		Analog Output (VOUT)
MSB	LSB	
1111	1111 1111 1111	+10 (65535/65536) V
1000	0000 0000 0000	+10 (32768/65536) V
0000	0000 0000 0001	+10 (1/65536) V
0000	0000 0000 0000	0

NOTE  
1 LSB = 10 V/2<sup>16</sup> = 10 V/65536 = 152 μV.

Offset and gain may be adjusted in Figure 18 as follows: To adjust offset, disconnect the VREF- input from 0 V, load the DAC with all 0s and adjust the VREF- voltage until VOUT = 0 V. For gain adjustment, the AD7846 should be loaded with all 1s and R1 adjusted until VOUT = 10 (65535)/(65536) = 9.999847 V. If a simple resistor divider is used to vary the VREF- voltage, it is important that the temperature coefficients of these resistors match that of the DAC input resistance (–300 ppm/°C). Otherwise, extra offset errors will be introduced over temperature. Many circuits will not require these offset and gain adjustments. In these circuits, R1 can be omitted. Pin 5 of the AD586 may be left open circuit and Pin 8 (VREF-) of the AD7846 tied to 0 V.

## BIPOLAR OPERATION

Figure 19 shows the AD7846 set up for  $\pm 10$  V bipolar operation. The AD588 provides precision  $\pm 5$  V tracking outputs which are fed to the  $V_{REF+}$  and  $V_{REF-}$  inputs of the AD7846. The code table for Figure 19 is shown in Table IV.

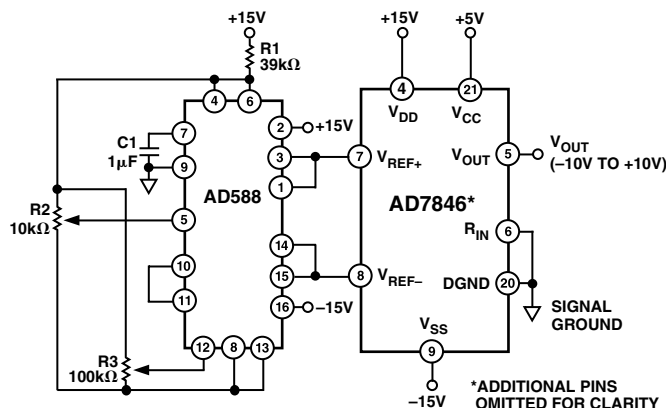


Figure 19. Bipolar  $\pm 10$  V Operation

Table IV. Offset Binary Code Table for Figure 19

Binary Number in DAC Latch	Analog Output ( $V_{OUT}$ )
MSB                      LSB	
1111 1111 1111 1111	+10 (32767/32768) V
1000 0000 0000 0001	+10 (1/32768) V
1000 0000 0000 0000	0 V
0111 1111 1111 1111	-10 (1/32768) V
0000 0000 0000 0000	-10 (32768/32768) V

### NOTE

1 LSB =  $10 \text{ V}/2^{15} = 10 \text{ V}/32768 = 305 \mu\text{V}$ .

Full scale and bipolar zero adjustment are provided by varying the gain and balance on the AD588. R2 varies the gain on the AD588 while R3 adjusts the +5 V and -5 V outputs together with respect to ground.

For bipolar zero adjustment on the AD7846, load the DAC with 100 . . . 000 and adjust R3 until  $V_{OUT} = 0$  V. Full scale is adjusted by loading the DAC with all 1s and adjusting R2 until  $V_{OUT} = 9.999694$  V.

When bipolar zero and full scale adjustment are not needed, R2 and R3 can be omitted, Pin 12 on the AD588 should be connected to Pin 11 and Pin 5 should be left floating. If a user wants a +5 V output range, there are two choices. By tying Pin 6 ( $R_{IN}$ ) of the AD7846 to  $V_{OUT}$  (Pin 5), the output stage gain is reduced to unity and the output range is  $\pm 5$  V. If only a positive +5 V reference is available, bipolar  $\pm 5$  V operation is still possible. Tie  $V_{REF-}$  to 0 V and connect  $R_{IN}$  to  $V_{REF+}$ . This will also give a  $\pm 5$  V output range. However, the linearity, gain, and offset error specifications will be the same as the unipolar 0 V to +5 V range.

## Other Output Voltage Ranges

In some cases, users may require output voltage ranges other than those already mentioned. One example is systems which need the output voltage to be a whole number of millivolts (i.e., 1 mV, 2 mV, etc.). If the AD689 (8.192 V reference) is used with the AD7846 as in Figure 20, then the LSB size is 125  $\mu\text{V}$ . This makes it possible to program whole millivolt values at the Output. Table V shows the code table for Figure 20.

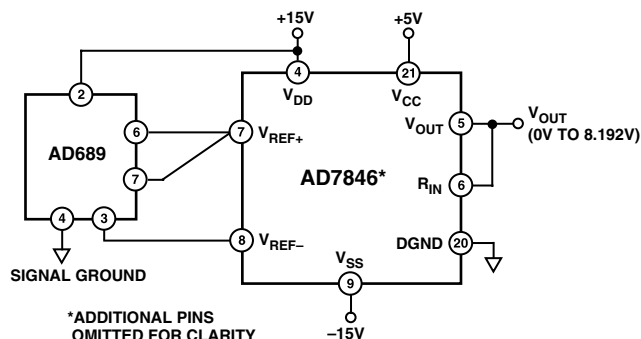


Figure 20. Unipolar Output with AD689

Table V. Code Table for Figure 20

Binary Number in DAC Latch	Analog Output ( $V_{OUT}$ )
MSB                      LSB	
1111 1111 1111 1111	8.192 V (65535/65536) = 8.1919 V
1000 0000 0000 0000	8.192 V (32768/65536) = 4.096 V
0000 0000 0000 1000	8.192 V (8/65536) = 0.001 V
0000 0000 0000 0100	8.192 V (4/65536) = 0.0005 V
0000 0000 0000 0010	8.192 V (2/65536) = 0.00025 V
0000 0000 0000 0001	8.192 V (1/65536) = 0.000125 V

### NOTE

1 LSB =  $8.192 \text{ V}/2^{16} = 125 \mu\text{V}$ .

## Multiplying Operation

The AD7846 is a full multiplying DAC. To get four-quadrant multiplication, tie  $V_{REF-}$  to 0 V, apply the ac input to  $V_{REF+}$  and tie  $R_{IN}$  to  $V_{REF+}$ . Figure 6 shows the Large Signal Frequency Response when the DAC is used in this fashion.

# AD7846

## TEST APPLICATION

Figure 21 shows the AD7846 in an Automatic Test Equipment application. The readback feature of the AD7846 is very useful in these systems. It allows the designer to eliminate phantom memory used for storing DAC contents and increases system reliability since the phantom memory is now effectively on chip with the DAC. The readback feature is used in the following manner to control a data transfer. First, write the desired 16-bit word to the DAC input latch using the  $\overline{\text{CS}}$  and  $\text{R}/\overline{\text{W}}$  inputs. Verify that correct data has been received by reading back the latch contents. Now, the data transfer can be completed by bringing the asynchronous  $\overline{\text{LDAC}}$  control line low. The analog equivalent of the digital word now appears at the DAC output. In Figure 21, each pin on the Device Under Test can be an

input or output. The AD345 is the pin driver for the digital inputs, and the AD9687 is the receiver for the digital outputs. The digital control circuitry determines the signal timing and format.

DACs 1 and 2 set the pin driver voltage levels ( $V_H$  and  $V_L$ ), and DACs 3 and 4 set the receiver voltage levels. The pin drivers used in ATE systems normally have a nonlinearity between input and output. The 16-bit resolution of the AD7846 allows compensation for these input/output nonlinearities. The dc parametrics shown in Figure 21 measure the voltage at the device pin and feed this back to the system processor. The pin voltage can thus be fine-tuned by incrementing or decrementing DACs 1 and 2 under system processor control.

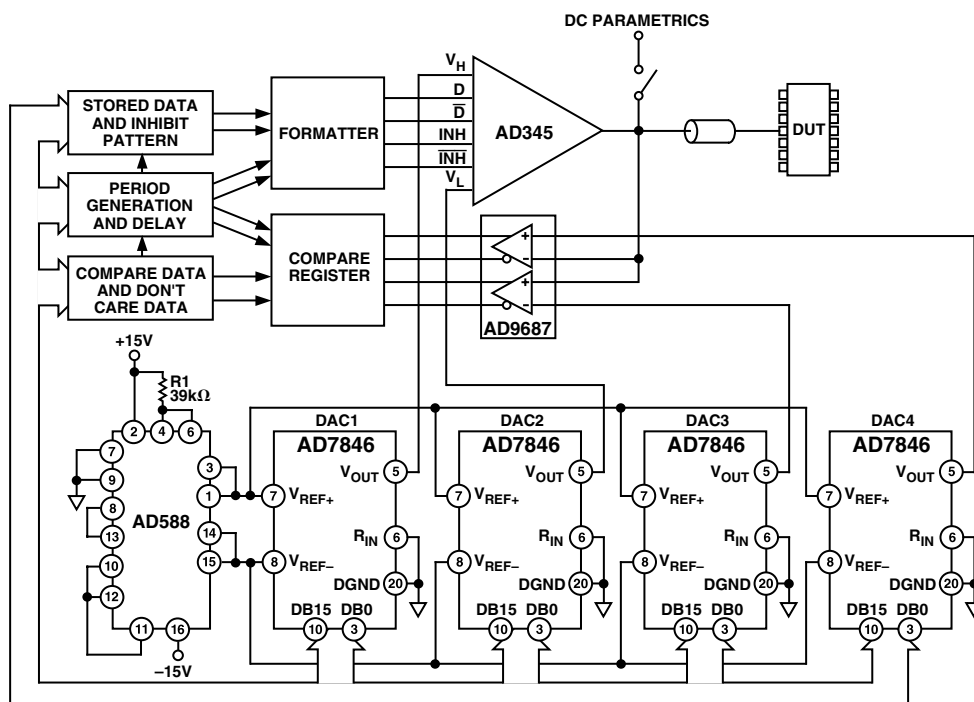
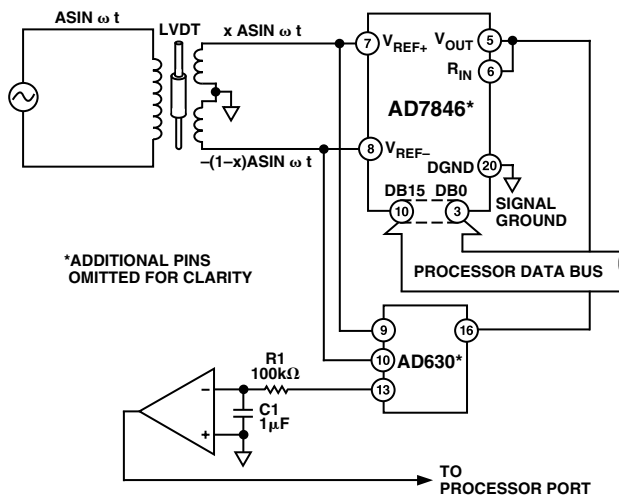


Figure 21. Digital Test System with 16-Bit Performance

## POSITION MEASUREMENT APPLICATION

Figure 22 shows the AD7846 in a position measurement application using an LVDT (Linear Variable Displacement Transducer), an AD630 synchronous demodulator and a comparator to make a 16-bit LVDT-to-Digital Converter. The LVDT is excited with a fixed frequency and fixed amplitude sine wave (usually 2.5 kHz, 2 V pk-pk). The outputs of the secondary coil are in antiphase and their relative amplitudes depend on the position of the core in the LVDT. The AD7846 output interpolates between these two inputs in response to the DAC input code. The AD630 is set up so that it rectifies the DAC output signal. Thus, if the output of the DAC is in phase with the  $V_{REF+}$  input, the inverting input to the comparator will be positive, and if it is in phase with  $V_{REF-}$ , the output will be negative. By turning on each bit of the DAC in succession starting with the MSB, and deciding to leave it on or turn it off based on the comparator output, a 16-bit measurement of the core position is obtained.



*Figure 22. AD7846 in Position Measurement Application*

## MICROPROCESSOR INTERFACING

## AD7846-to-8086 Interface

Figure 23 shows the 8086 16-bit processor interfacing to the AD7846. The double buffering feature of the DAC is not used in this circuit since LDAC is permanently tied to 0 V. AD0–AD15 (the 16-bit data bus) are connected to the DAC data bus (DB0–DB15). The 16-bit word is written to the DAC in one MOV instruction and the analog output responds immediately. In this example, the DAC address is D000H.

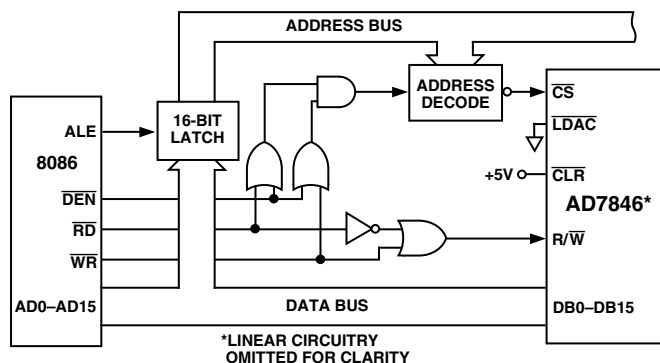


Figure 23. AD7846-to-8086 Interface Circuit

In a multiple DAC system, the double buffering of the AD7846 allows the user to simultaneously update all DACs. In Figure 24, a 16-bit word is loaded to the input latches of each of the DACs in sequence. Then, with one instruction to the appropriate address, CS4 (i.e.,  $\overline{\text{LDAC}}$ ) is brought low, updating all the DACs simultaneously.

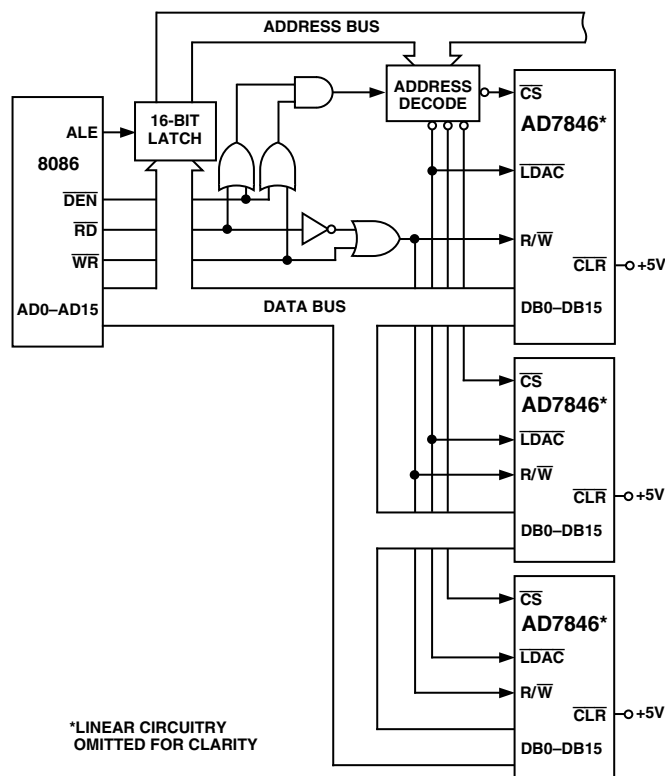


Figure 24. AD7846-to-8086 Interface: Multiple DAC System

## AD7846-to-MC68000 Interface

Interfacing between the AD7846 and MC68000 is accomplished using the circuit of Figure 25. The following routine writes data to the DAC latches and then outputs the data via the DAC latch.

1000	MOVE.W #W, D0	The desired DAC data, W, is loaded into Data Register 0. W may be any value between 0 and 65535 (decimal) or 0 and FFFF (hexadecimal).
------	---------------	--

MOVE.W	D0, \$E000	The data, W, is transferred between D0 and the DAC register.
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MOVE.W	#228, D7	Control is returned to the
TRAP	#14	System Monitor using
		these two instructions.

# AD7846

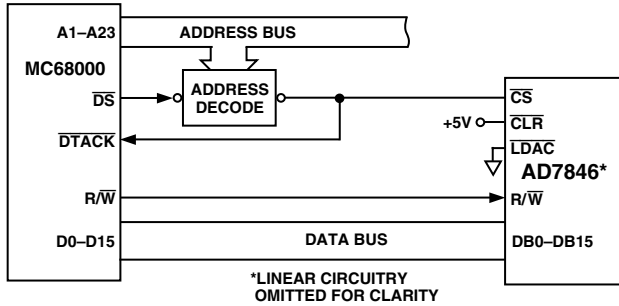


Figure 25. AD7846-to-MC68000 Interface

## DIGITAL FEEDTHROUGH

In the preceding interface configurations, most digital inputs to the AD7846 are directly connected to the microprocessor bus. Even when the device is not selected, these inputs will be constantly changing. The high frequency logic activity on the bus can feed through the DAC package capacitance to show up as noise on the analog output. To minimize this Digital Feedthrough isolate the DAC from the noise source. Figure 26 shows an interface circuit which isolates the DAC from the bus.

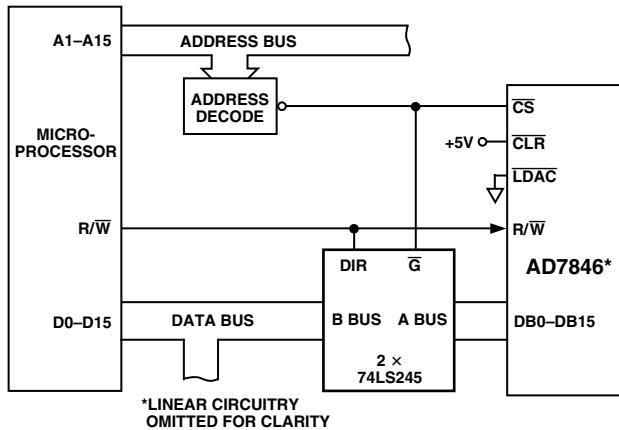


Figure 26. AD7846 Interface Circuit Using Latches to Minimize Digital Feedthrough

Note that to make use of the AD7846 readback feature using the isolation technique of Figure 26, the latch needs to be bidirectional.

## APPLICATION HINTS

### Noise

In high resolution systems, noise is often the limiting factor. With a 10 volt span, a 16-bit LSB is 152  $\mu$ V (–96 dB). Thus, the noise floor must stay below –96 dB in the frequency range of interest. Figure 7 shows the noise spectral density for the AD7846.

### Grounding

As well as noise, the other prime consideration in high resolution DAC systems is grounding. With an LSB size of 152  $\mu$ V and a load current of 5 mA, 1 LSB of error can be introduced by series resistance of only 0.03  $\Omega$ .

Figure 27 below shows recommended grounding for the AD7846 in a typical application.

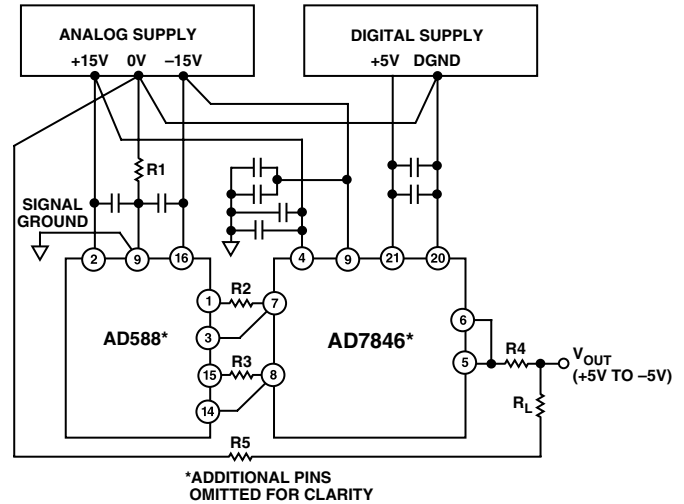


Figure 27. AD7846 Grounding

R1 to R5 represent lead and track resistances on the printed circuit board. R1 is the resistance between the Analog Power Supply ground and the Signal Ground. Since current flowing in R1 is very low (bias current of AD588 sense amplifier), the effect of R1 is negligible. R2 and R3 represent track resistance between the AD588 outputs and the AD7846 reference inputs. Because of the Force and Sense outputs on the AD588, these resistances will also have a negligible effect on accuracy.

R4 is the resistance between the DAC output and the load. If  $R_L$  is constant, then R4 will introduce a gain error only which can be trimmed out in the calibration cycle. R5 is the resistance between the load and the analog common. If the output voltage is sensed across the load, R5 will introduce a further gain error which can be trimmed out. If, on the other hand, the output voltage is sensed at the analog supply common, R5 appears as part of the load and therefore introduces no errors.

### Printed Circuit Board Layout

Figure 28 shows the AD7846 in a typical application with the AD588 reference, producing an output analog voltage in the  $\pm 10$  volts range. Full scale and bipolar zero adjustment are provided by potentiometers R2 and R3. Latches ( $2 \times 74LS245$ ) isolate the DAC digital inputs from the active microprocessor bus and minimize digital feedthrough.

The printed circuit board layout for Figure 28 is shown in Figures 29 and 30. Figure 29 is the component side layout while Figure 30 is the solder side layout. The component overlay is shown in Figure 31.

In the layout, the general grounding guidelines given in Figure 27 are followed. The AD588 and AD7846 are as close as possible, and the decoupling capacitors for these are also kept as close to the device pins as possible.

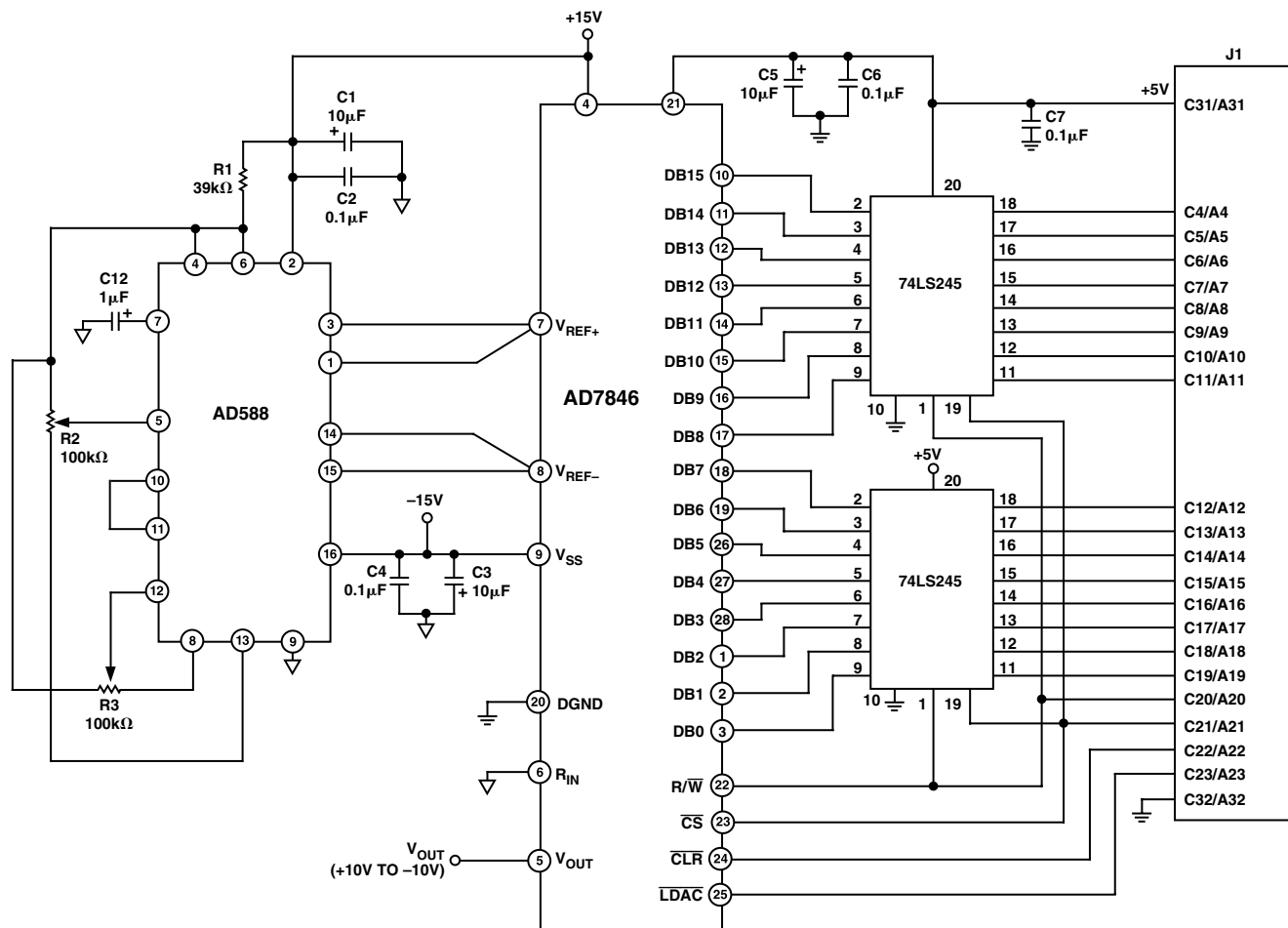


Figure 28. Schematic for AD7846 Board

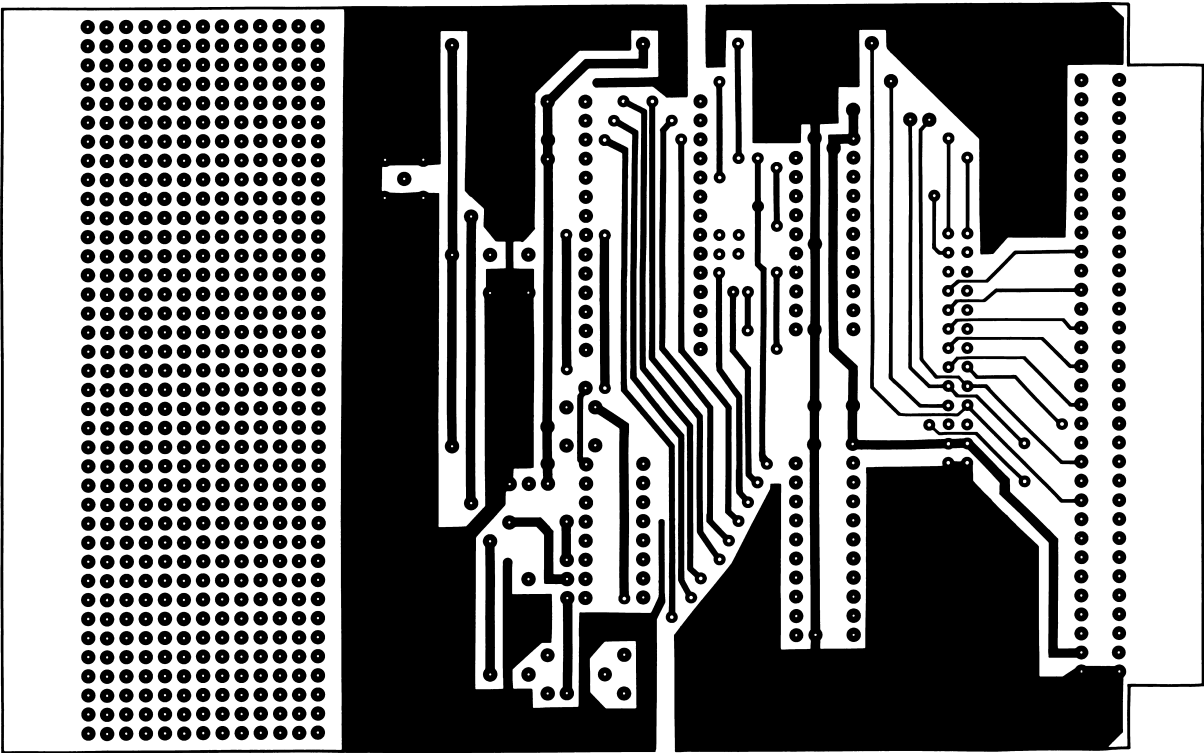


Figure 29. PCB Component Side Layout for Figure 28

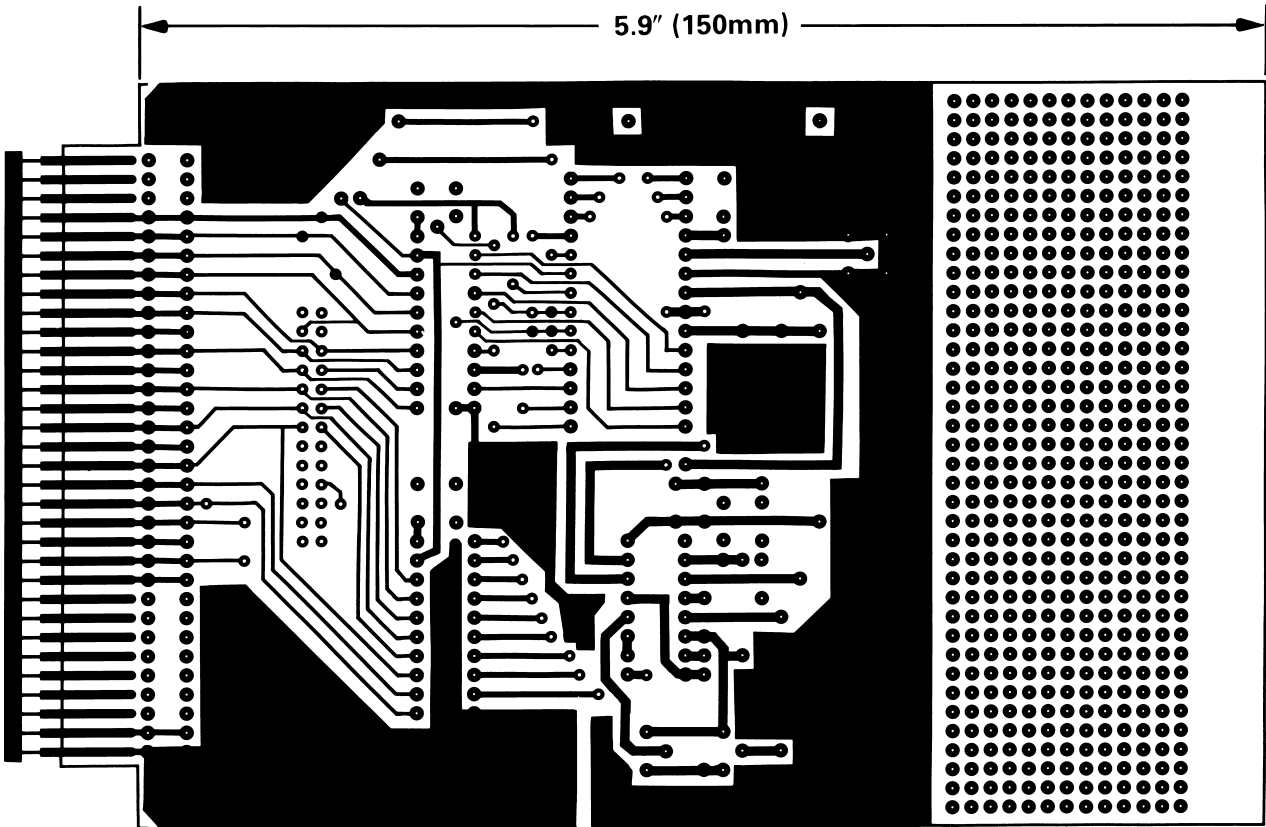


Figure 30. PCB Solder Side Layout for Figure 30

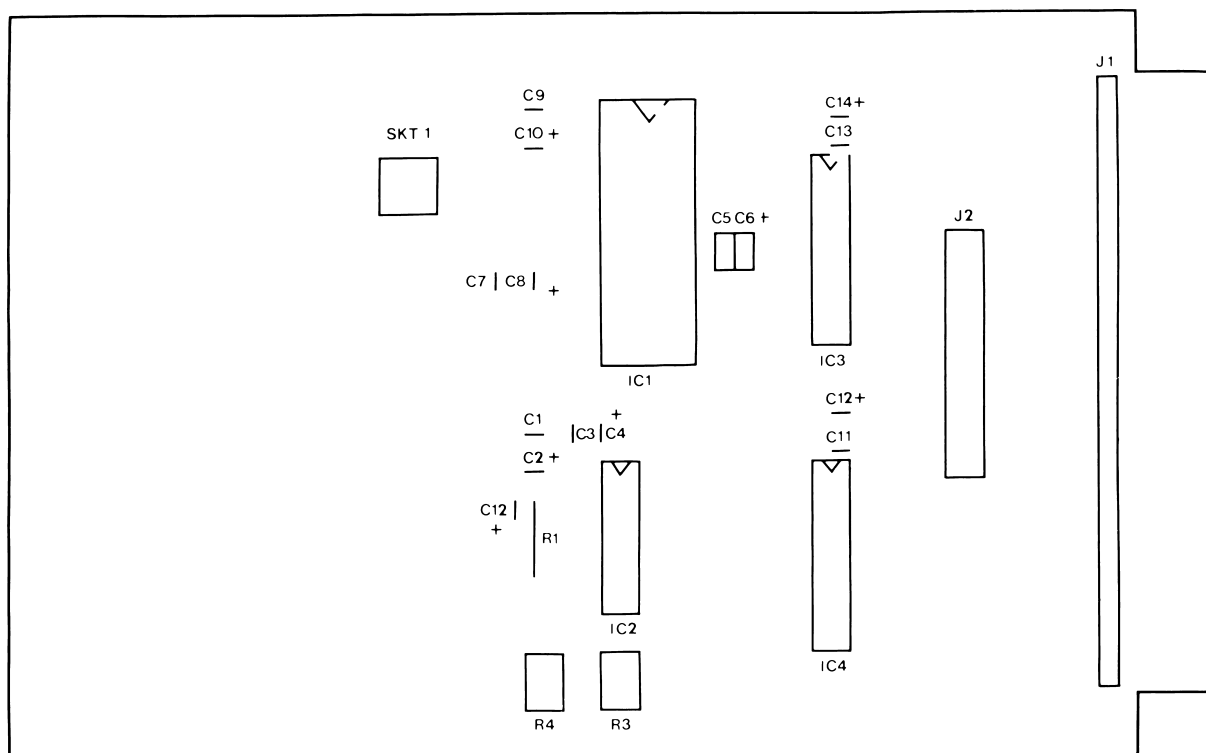
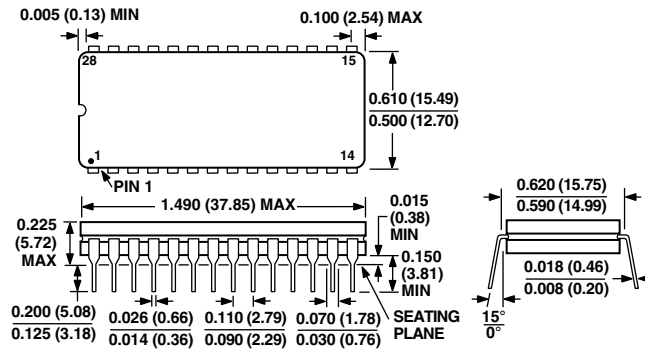


Figure 31. Component Overlay for Circuit of Figure 28

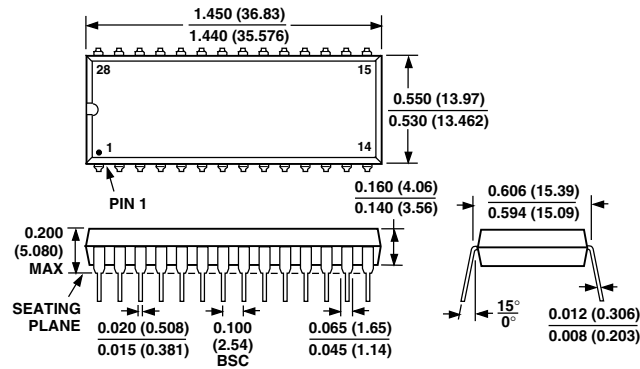
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

## 28-Lead Ceramic DIP (Q-28)



## 28-Lead Plastic DIP (N-28A)

28-Lead Plastic Leaded Chip Carrier (PLCC)  
(P-28A)