

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT390** Dual decade ripple counter

Product specification  
File under Integrated Circuits, IC06

December 1990

## Dual decade ripple counter

## 74HC/HCT390

## FEATURES

- Two BCD decade or bi-quinary counters
- One package can be configured to divide-by-2, 4, 5, 10, 20, 25, 50 or 100
- Two master reset inputs to clear each decade counter individually
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT390 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT390 are dual 4-bit decade ripple counters divided into four separately clocked sections. The counters have two divide-by-2 sections and two divide-by-5 sections. These sections are normally used in a BCD

decade or bi-quinary configuration, since they share a common master reset input (nMR). If the two master reset inputs (1MR and 2MR) are used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clocks ( $\overline{nCP_0}$  and  $\overline{nCP_1}$ ) of each section allow ripple counter or frequency division applications of divide-by-2, 4, 5, 10, 20, 25, 50 or 100.

Each section is triggered by the HIGH-to-LOW transition of the clock inputs ( $\overline{nCP_0}$  and  $\overline{nCP_1}$ ). For BCD decade operation, the nQ<sub>0</sub> output is connected to the  $\overline{nCP_1}$  input of, the divide-by-5 section. For bi-quinary decade operation, the nQ<sub>3</sub> output is connected to the  $\overline{nCP_0}$  input and nQ<sub>0</sub> becomes the decade output.

The master reset inputs (1MR and 2MR) are active HIGH asynchronous inputs to each decade counter which operates on the portion of the counter identified by the "1" and "2" prefixes in the pin configuration. A HIGH level on the nMR input overrides the clocks and sets the four outputs LOW.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay n $\overline{CP_0}$ to nQ <sub>0</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	14	18	ns
	n $\overline{CP_1}$ to nQ <sub>1</sub>		15	19	ns
	n $\overline{CP_1}$ to nQ <sub>2</sub>		23	26	ns
	n $\overline{CP_1}$ to nQ <sub>3</sub>		15	19	ns
	nMR to Q <sub>n</sub>		16	18	ns
f <sub>max</sub>	maximum clock frequency $\overline{nCP_0}$ , $\overline{nCP_1}$		66	61	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per counter	notes 1 and 2	20	21	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> -1.5 V

Dual decade ripple counter

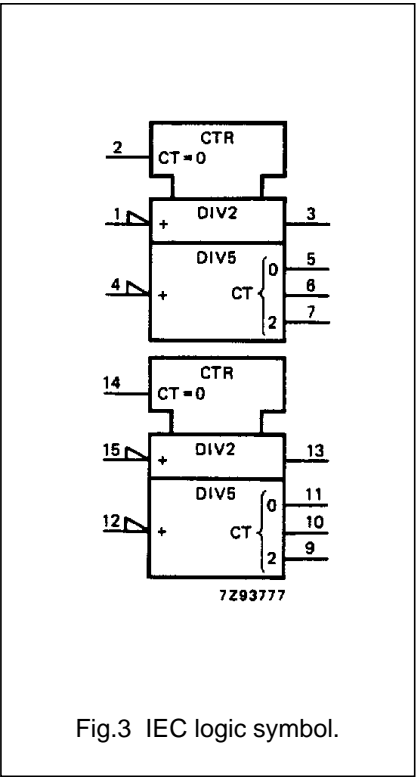
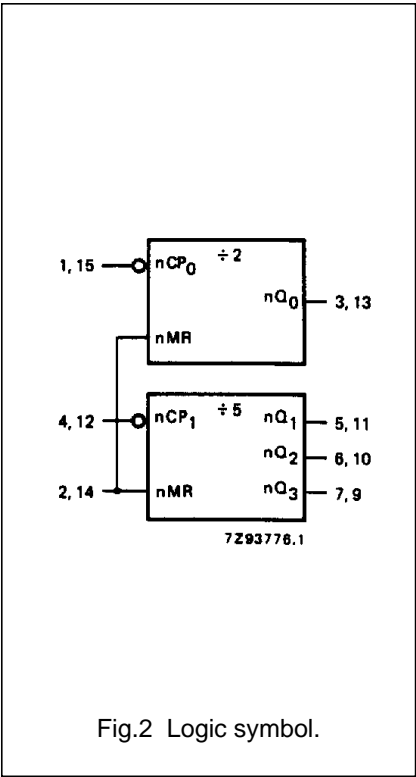
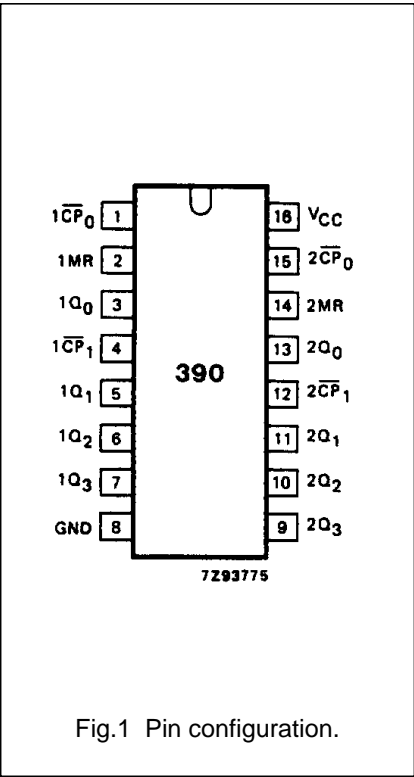
74HC/HCT390

ORDERING INFORMATION

See “74HC/HCT/HCU/HCMOS Logic Package Information”.

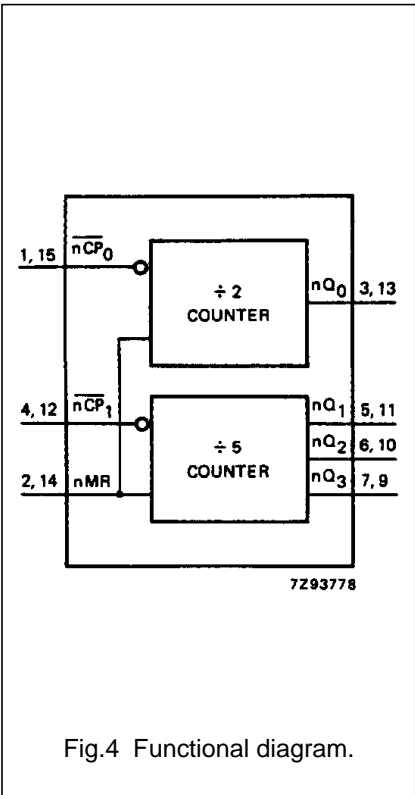
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{CP}_0, 2\overline{CP}_0$	clock input divide-by-2 section (HIGH-to-LOW, edge-triggered)
2, 14	1MR, 2MR	asynchronous master reset inputs (active HIGH)
3, 5, 6, 7	$1Q_0$ to $1Q_3$	flip-flop outputs
4, 12	$1\overline{CP}_1, 2\overline{CP}_1$	clock input divide-by-5 section (HIGH-to-LOW, edge triggered)
8	GND	ground (0 V)
13, 11, 10, 9	$2Q_0$ to $2Q_3$	flip-flop outputs
16	$V_{CC}$	positive supply voltage



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BCD COUNT SEQUENCE  
FOR 1/2 THE “390”

COUNT	OUTPUTS			
	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

Notes

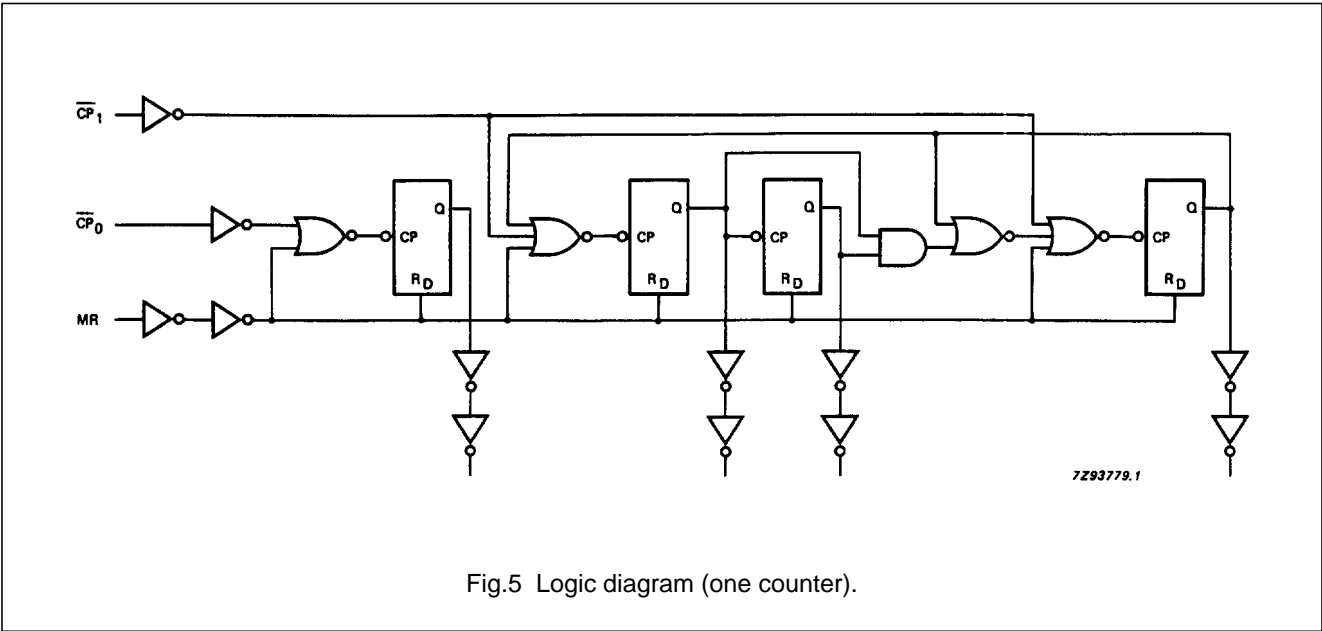
- 1. Output Q<sub>0</sub> connected to  $\overline{nCP_1}$  with counter input on  $\overline{nCP_0}$ .  
H = HIGH voltage level  
L = LOW voltage level

BI-QUINARY COUNT SEQUENCE  
FOR 1/2 THE “390”

COUNT	OUTPUTS			
	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	L	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

Note

- 1. Output Q<sub>3</sub> connected to  $\overline{nCP_0}$  with counter input on  $\overline{nCP_1}$ .



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## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>0</sub> to nQ <sub>0</sub>		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>1</sub> to nQ <sub>1</sub>		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>1</sub> to nQ <sub>2</sub>		74 27 22	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>1</sub> to nQ <sub>3</sub>		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub>	propagation delay nMR to nQ <sub>n</sub>		52 19 15	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig.7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t <sub>W</sub>	clock pulse width nCP <sub>0</sub> , nCP <sub>1</sub>	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t <sub>W</sub>	master reset pulse width HIGH	80 17 14	28 10 8		105 21 18		130 26 22		ns	2.0 4.5 6.0	Fig.7
t <sub>rem</sub>	removal time nMR to nCP <sub>n</sub>	75 15 13	22 8 6		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig.7
f <sub>max</sub>	maximum clock pulse frequency nCP <sub>0</sub> , nCP <sub>1</sub>	6.0 30 35	20 60 71		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.6

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{nCP_0}$	0.45
$\overline{nCP_1}$ , nMR	0.60

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HCT								V <sub>CC</sub> (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>0</sub> to nQ <sub>0</sub>		21	34		43		51	ns	4.5	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>1</sub> to nQ <sub>1</sub>		22	38		48		57	ns	4.5	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>1</sub> to nQ <sub>2</sub>		30	51		64		77	ns	4.5	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP <sub>1</sub> to nQ <sub>3</sub>		22	38		48		57	ns	4.5	Fig.6
t <sub>PHL</sub>	propagation delay nMR to nQ <sub>n</sub>		21	36		45		54	ns	4.5	Fig.7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.6
t <sub>W</sub>	clock pulse width nCP <sub>0</sub> , nCP <sub>1</sub>	18	8		23		27		ns	4.5	Fig.6
t <sub>W</sub>	master reset pulse width HIGH	17	10		21		26		ns	4.5	Fig.7
t <sub>rem</sub>	removal time nMR to nCP <sub>n</sub>	15	8		19		22		ns	4.5	Fig.7
f <sub>max</sub>	maximum clock pulse frequency nCP <sub>0</sub> , nCP <sub>1</sub>	27	55		22		18		MHz	4.5	Fig.6

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## AC WAVEFORMS

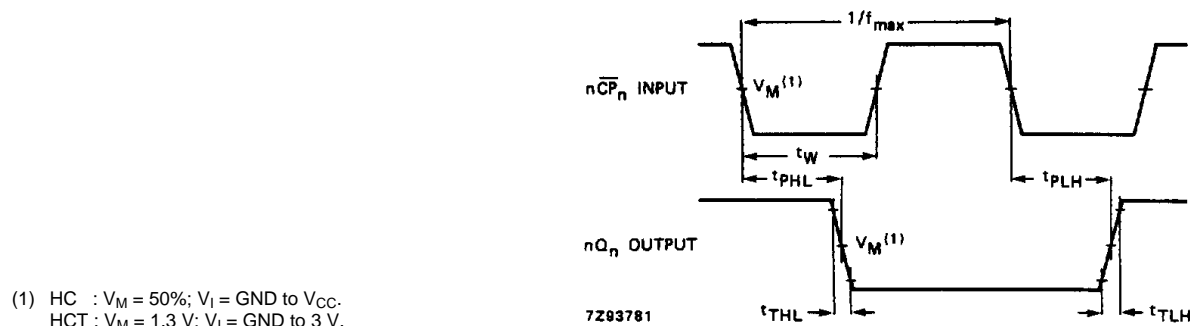


Fig.6 Waveforms showing the clock ( $\overline{nCP_n}$ ) to output ( $nQ_n$ ) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

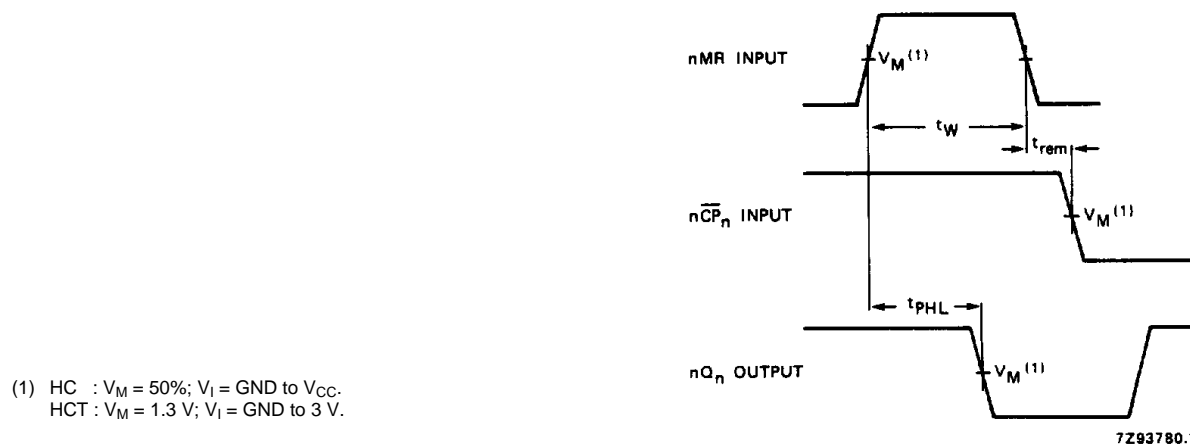


Fig.7 Waveforms showing the master reset ( $nMR$ ) pulse width, the master reset to output ( $nQ_n$ ) propagation delays and the master reset to clock ( $\overline{nCP_n}$ ) removal time.

## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".