

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT125

Quad buffer/line driver; 3-state

Product specification
File under Integrated Circuits, IC06

December 1990

Quad buffer/line driver; 3-state**74HC/HCT125****FEATURES**

- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT125 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT125 are four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (nOE). A HIGH at nOE causes the outputs to assume a HIGH impedance OFF-state.

The “125” is identical to the “126” but has active LOW enable inputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------------------------|--|---|---------|-----|------|
| | | | HC | HCT | |
| t _{PHL} / t _{PLH} | propagation delay nA to nY | C _L = 15 pF; V _{CC} = 5 V | 9 | 12 | ns |
| C _I | input capacitance | | 3.5 | 3.5 | pF |
| C _{PD} | power dissipation capacitance per buffer | notes 1 and 2 | 22 | 24 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

∑ (C_L × V_{CC}² × f_o) = sum of outputs

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See “74HC/HCT/HCU/HCMOS Logic Package Information”.

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PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|--------------|--------------------------------------|------------------------------------|
| 1, 4, 10, 13 | $\overline{1OE}$ to $\overline{4OE}$ | outputs enable inputs (active LOW) |
| 2, 5, 9, 12 | 1A to 4A | data inputs |
| 3, 6, 8, 11 | 1Y to 4Y | data outputs |
| 7 | GND | ground (0 V) |
| 14 | V _{CC} | positive supply voltage |

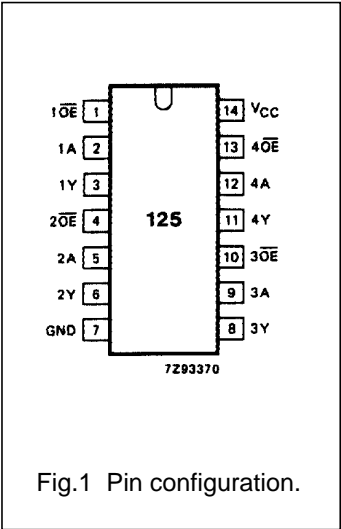


Fig.1 Pin configuration.

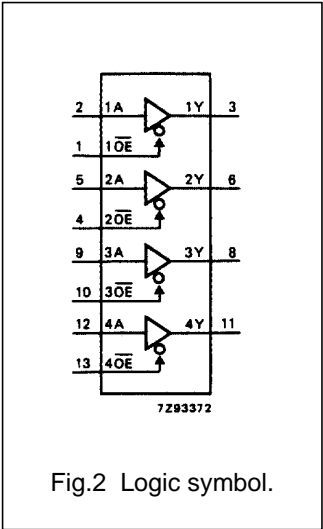


Fig.2 Logic symbol.

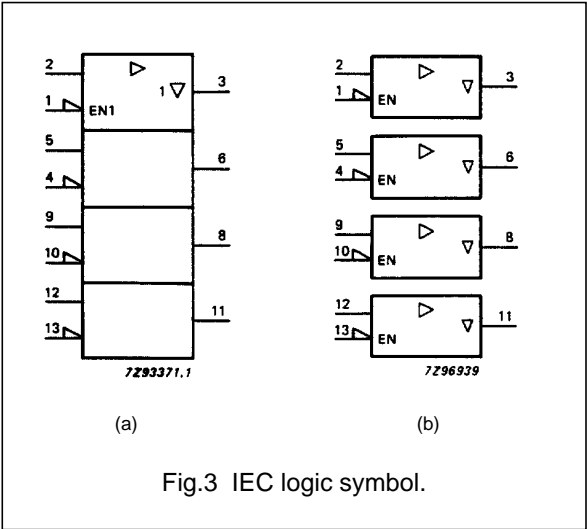


Fig.3 IEC logic symbol.

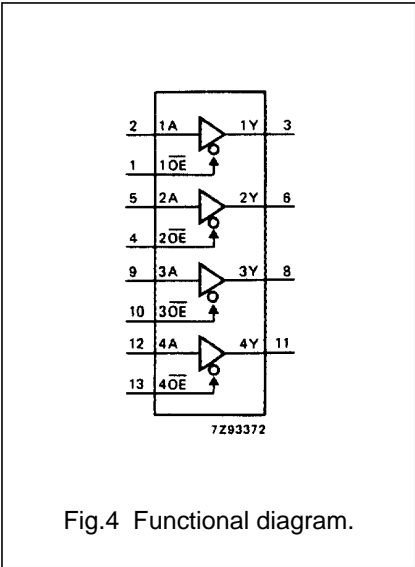


Fig.4 Functional diagram.

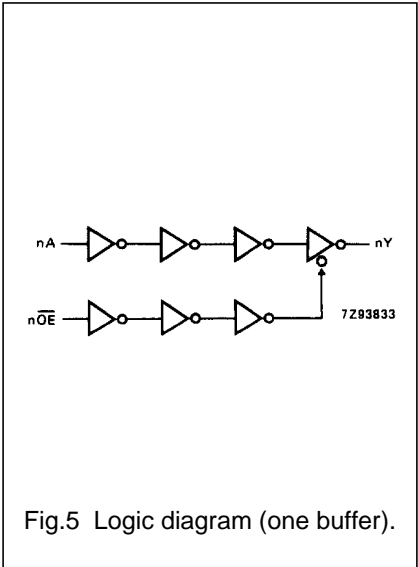


Fig.5 Logic diagram (one buffer).

FUNCTION TABLE

| INPUTS | | OUTPUT |
|------------------|----|--------|
| \overline{nOE} | nA | nY |
| L | L | L |
| L | H | H |
| H | X | Z |

- Note**
1. H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|-------------------------------------|---|-----------------------|----------------|-----------------|------------|-----------------|-------------|-----------------|------|------------------------|-----------|
| | | 74HC | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| t _{PHL} / t _{PLH} | propagation delay nA to nY | | 30 11 9 | 100 20 17 | | 125 25 21 | | 150 30 26 | ns | 2.0 4.5 6.0 | Fig.6 |
| t _{PZH} / t _{PZL} | 3-state output enable time n $\overline{\text{OE}}$ to nY | | 41 15 12 | 125 25 21 | | 155 31 26 | | 190 38 32 | ns | 2.0 4.5 6.0 | Fig.7 |
| t _{PHZ} / t _{PLZ} | 3-state output disable time n $\overline{\text{OE}}$ to nY | | 41 15 12 | 125 25 21 | | 155 31 26 | | 190 38 32 | ns | 2.0 4.5 6.0 | Fig.7 |
| t _{THL} / t _{TLH} | output transition time | | 14 5 4 | 60 12 10 | | 75 15 13 | | 90 18 15 | ns | 2.0 4.5 6.0 | Fig.6 |

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|-----------------------|-----------------------|
| nA, n \overline{OE} | 1.00 |

AC CHARACTERISTICS FOR 74HCT

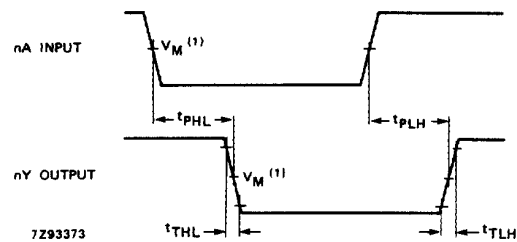
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|-------------------------------------|--|-----------------------|------|------|------------|------|-------------|------|------|------------------------|-----------|
| | | 74HCT | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| t _{PHL} / t _{PLH} | propagation delay nA to nY | | 15 | 25 | | 31 | | 38 | ns | 4.5 | Fig.6 |
| t _{PZH} / t _{PZL} | 3-state output enable time n \overline{OE} to nY | | 15 | 28 | | 35 | | 42 | ns | 4.5 | Fig.7 |
| t _{PHZ} / t _{PLZ} | 3-state output disable time n \overline{OE} to nY | | 15 | 25 | | 31 | | 38 | ns | 4.5 | Fig.7 |
| t _{THL} / t _{TLH} | output transition time | | 5 | 12 | | 15 | | 18 | ns | 4.5 | Fig.6 |

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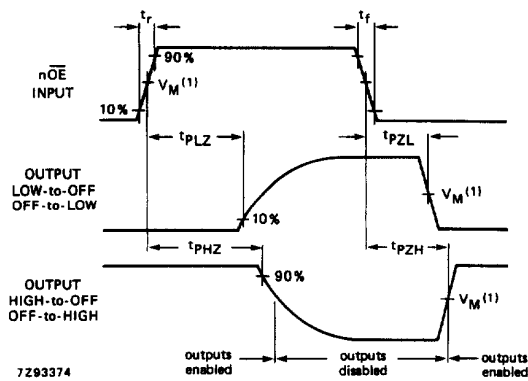
74HC/HCT125

AC WAVEFORMS



- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 HCT : $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.6 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.



- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 HCT : $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.7 Waveforms showing the 3-state enable and disable times.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".