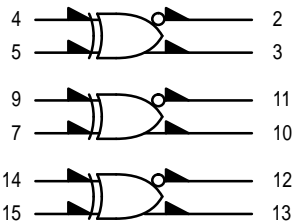


Triple 2-Input Exclusive OR/ Exclusive NOR Gate

The MC10107 is a triple-2 input exclusive OR/NOR gate.

$P_D = 40 \text{ mW typ/gate (No Load)}$
 $t_{pd} = 2.8 \text{ ns typ}$
 $t_r, t_f = 2.5 \text{ ns typ (20\%--80\%)}$

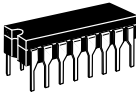
LOGIC DIAGRAM



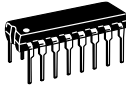
$$3 = (4 \bullet \overline{5}) + (\overline{4} \bullet 5)$$
$$2 = (4 \bullet 5) + (\overline{4} \bullet \overline{5})$$

$V_{CC1} = \text{PIN } 1$
 $V_{CC2} = \text{PIN } 16$
 $V_{EE} = \text{PIN } 8$

MC10107



L SUFFIX
CERAMIC PACKAGE
CASE 620-10

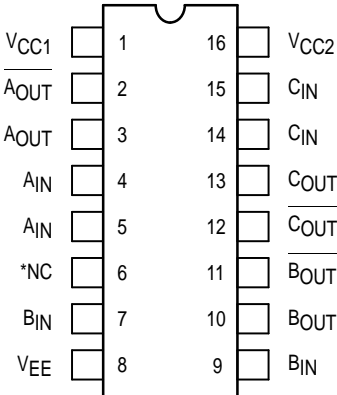


P SUFFIX
PLASTIC PACKAGE
CASE 648-08



FN SUFFIX
PLCC
CASE 775-02

DIP PIN ASSIGNMENT



*NC = No Connection

Pin assignment is for Dual-in-Line Package.
For PLCC pin assignment, see the Pin Conversion
Tables on page 6-11 of the Motorola MECL Data
Book (DL122/D).



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			−30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I _E	8		31			28		31	mAdc
Input Current	I _{inH}	4, 9, 14 5, 7, 15		425 350			265 220		265 220	μAdc
	I _{inL}	*	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V _{OH}	2 2 3 3	−1.060 −1.060 −1.060 −1.060	−0.890 −0.890 −0.890 −0.890	−0.960 −0.960 −0.960 −0.960		−0.810 −0.810 −0.810 −0.810	−0.890 −0.890 −0.890 −0.890	−0.700 −0.700 −0.700 −0.700	Vdc
Output Voltage Logic 0	V _{OL}	2 2 3 3	−1.890 −1.890 −1.890 −1.890	−1.675 −1.675 −1.675 −1.675	−1.850 −1.850 −1.850 −1.850		−1.650 −1.650 −1.650 −1.650	−1.825 −1.825 −1.825 −1.825	−1.615 −1.615 −1.615 −1.615	Vdc
Threshold Voltage Logic 1	V _{OHA}	2 2 3 3	−1.080 −1.080 −1.080 −1.080		−0.980 −0.980 −0.980 −0.980			−0.910 −0.910 −0.910 −0.910		Vdc
Threshold Voltage Logic 0	V _{OLA}	2 2 3 3		−1.655 −1.655 −1.655 −1.655			−1.630 −1.630 −1.630 −1.630		−1.595 −1.595 −1.595 −1.595	Vdc
Switching Times (50Ω Load)					Min	Typ	Max			ns
Propagation Delay	t ₊₊	Inputs	−1.1	3.8	1.1	2.0	3.7	1.1	4.0	
	t _{+ −}	4,9 or 14	1.1	3.8	1.1	2.0	3.7	1.1	4.0	
	t _{−+}	to either	1.1	3.8	1.1	2.0	3.7	1.1	4.0	
	t _{− −}	Output	1.1	3.8	1.1	2.0	3.7	1.1	4.0	
	t ₊₊	Inputs	1.1	3.8	1.1	2.8	3.7	1.1	4.0	
	t _{+ −}	5,7 or 15	1.1	3.8	1.1	2.8	3.7	1.1	4.0	
	t _{−+}	to either	1.1	3.8	1.1	2.8	3.7	1.1	4.0	
	t _{− −}	Output	1.1	3.8	1.1	2.8	3.7	1.1	4.0	
Rise Time (20 to 80%)	t ₊	**	1.1	3.5	1.1	2.5	3.5	1.1	3.8	
Fall Time (20 to 80%)	t _−	**	1.1	3.5	1.1	2.5	3.5	1.1	3.8	

* Individually test each input applying V_{IH} or V_{IL} to input under test.

** Any Output.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					(V _{CC}) Gnd
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}	
			−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
			+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
			+85°C	−0.700	−1.825	−1.035	−1.440	−5.2
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V _{CC}) Gnd
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}	
Power Supply Drain Current	I _E	8	5, 7, 15				8	1, 16
Input Current	I _{inH}	4, 9, 14 5, 7, 15	*				8	1, 16
	I _{inL}	*		*			8	1, 16
Output Voltage Logic 1	V _{OH}	2	4, 5				8	1, 16
		2					8	1, 16
		3	4				8	1, 16
		3	5				8	1, 16
Output Voltage Logic 0	V _{OL}	2	4				8	1, 16
		2	5				8	1, 16
		3	4, 5				8	1, 16
		3					8	1, 16
Threshold Voltage Logic 1	V _{OHA}	2	5		4		8	1, 16
		2				4	8	1, 16
		3			4		8	1, 16
		3			5		8	1, 16
Threshold Voltage Logic 0	V _{OLA}	2			4		8	1, 16
		2			5		8	1, 16
		3	5		4		8	1, 16
		3				4	8	1, 16
Switching Times (50Ω Load)			+1.1V		Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t ₊₊	Inputs	5, 7, 15		Input	Corresponding	8	1, 16
	t ₊₋	4,9 or 14	5, 7, 15		4, 9 or	XOR/XNOR	8	1, 16
	t ₋₊	to either	5, 7, 15		14	Outputs	8	1, 16
	t ₋₋	Output	5, 7, 15				8	1, 16
	t ₊₊	Inputs	4, 9, 14		Input	Corresponding	8	1, 16
	t ₊₋	5,7 or 15	4, 9, 14		5, 7 or	XOR/XNOR	8	1, 16
	t ₋₊	to either	4, 9, 14		15	Outputs	8	1, 16
	t ₋₋	Output	4, 9, 14				8	1, 16
Rise Time (20 to 80%)	t ₊	**	4, 9, 14		Any Input	Corresponding	8	1, 16
Fall Time (20 to 80%)	t ₋	**	4, 9, 14		Any Input	XOR/XNOR	8	1, 16

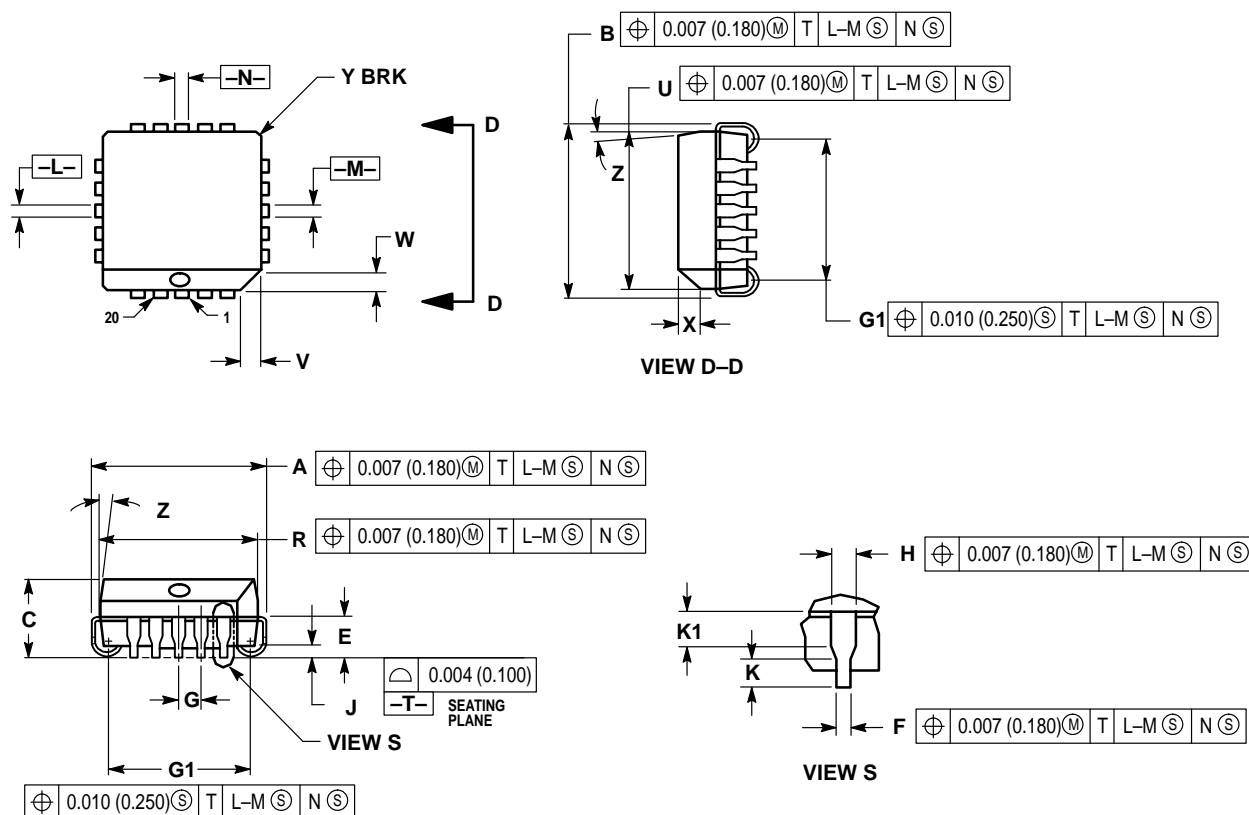
* Individually test each input applying V_{IH} or V_{IL} to input under test.

** Any Output.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

OUTLINE DIMENSIONS

FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775-02
ISSUE C



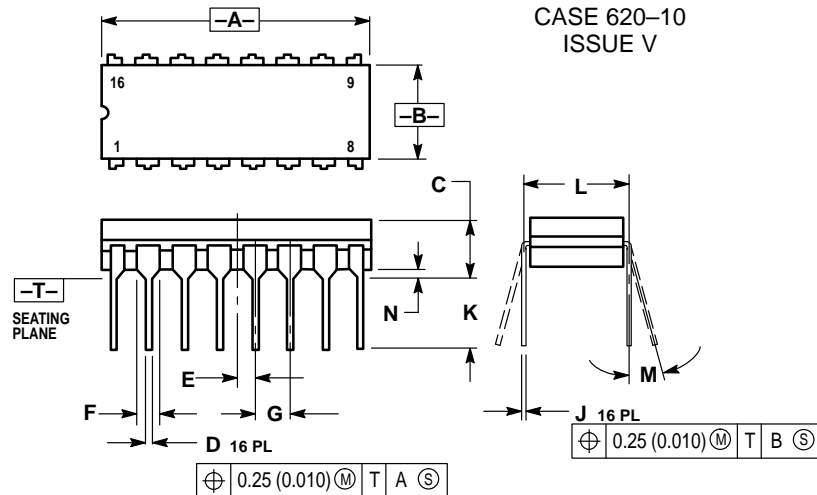
NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

OUTLINE DIMENSIONS

L SUFFIX
CERAMIC DIP PACKAGE
CASE 620-10
ISSUE V

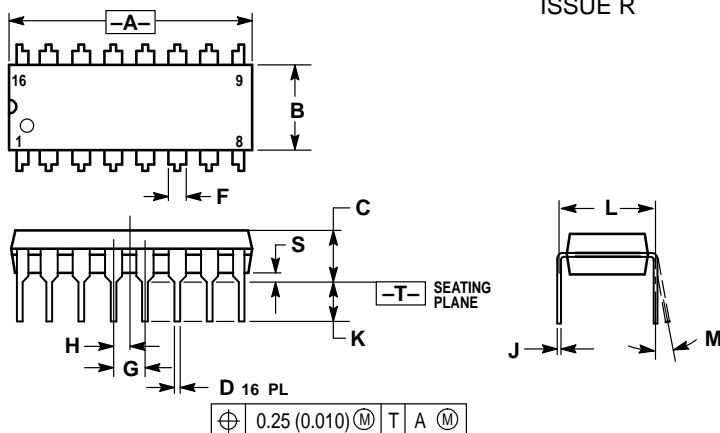


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01


P SUFFIX
PLASTIC DIP PACKAGE
CASE 648-08
ISSUE R



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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