

W27C512



64K × 8 ELECTRICALLY ERASABLE EPROM

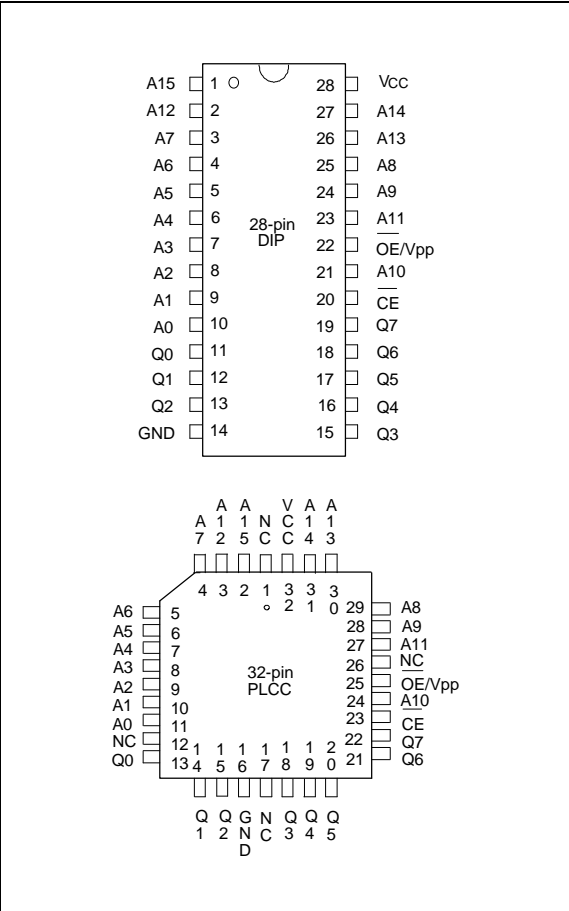
GENERAL DESCRIPTION

The W27C512 is a high speed, low power Electrically Erasable and Programmable Read Only Memory organized as 65536 × 8 bits that operates on a single 5 volt power supply. The W27C512 provides an electrical chip erase function.

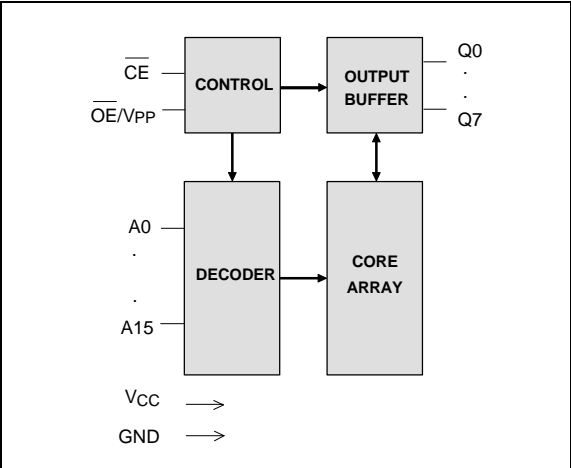
FEATURES

- High speed access time: 45/70/90/120 nS (max.)
- Read operating current: 30 mA (max.)
- Erase/Programming operating current 30 mA (max.)
- Standby current: 1 mA (max.)
- Single 5V power supply
- +14V erase/+12V programming voltage
- Fully static operation
- All inputs and outputs directly TTL/CMOS compatible
- Three-state outputs
- Available packages: 28-pin 600 mil DIP, 330 mil 32-pin PLCC

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A15	Address Inputs
Q0–Q7	Data Inputs/Outputs
\overline{CE}	Chip Enable
\overline{OE}/V_{PP}	Output Enable, Program/Erase Supply Voltage
VCC	Power Supply
GND	Ground
NC	No Connection



FUNCTIONAL DESCRIPTION

Read Mode

Like conventional UVEPROMs, the W27C512 has two control functions, both of which produce data at the outputs. \overline{CE} is for power control and chip select. \overline{OE}/VPP controls the output buffer to gate data to the output pins. When addresses are stable, the address access time (T_{ACC}) is equal to the delay from \overline{CE} to output (T_{CE}), and data are available at the outputs T_{OE} after the falling edge of \overline{OE}/VPP , if T_{ACC} and T_{CE} timings are met.

Erase Mode

The erase operation is the only way to change data from "0" to "1." Unlike conventional UVEPROMs, which use ultraviolet light to erase the contents of the entire chip (a procedure that requires up to half an hour), the W27C512 uses electrical erasure. Generally, the chip can be erased within 100 mS by using an EPROM writer with a special erase algorithm.

Erase mode is entered when \overline{OE}/VPP is raised to V_{PE} (14V), $V_{CC} = V_{CE}$ (5V), $A_9 = V_{PE}$ (14V), A_0 low, and all other address pins low and data input pins high. Pulsing \overline{CE} low starts the erase operation.

Erase Verify Mode

After an erase operation, all of the bytes in the chip must be verified to check whether they have been successfully erased to "1" or not. The erase verify mode ensures a substantial erase margin if $V_{CC} = V_{CE}$ (3.75V), \overline{CE} low, and \overline{OE}/VPP low.

Program Mode

Programming is performed exactly as it is in conventional UVEPROMs, and programming is the only way to change cell data from "1" to "0." The program mode is entered when \overline{OE}/VPP is raised to V_{PP} (12V), $V_{CC} = V_{CP}$ (5V), the address pins equal the desired addresses, and the input pins equal the desired inputs. Pulsing \overline{CE} low starts the programming operation.

Program Verify Mode

All of the bytes in the chip must be verified to check whether they have been successfully programmed with the desired data or not. Hence, after each byte is programmed, a program verify operation should be performed. The program verify mode automatically ensures a substantial program margin. This mode will be entered after the program operation if \overline{OE}/VPP low and \overline{CE} low.

Erase/Program Inhibit

Erase or program inhibit mode allows parallel erasing or programming of multiple chips with different data. When \overline{CE} high, erasing or programming of non-target chips is inhibited, so that except for the \overline{CE} and \overline{OE}/VPP pins, the W27C512 may have common inputs.



Standby Mode

The standby mode significantly reduces VCC current. This mode is entered when $\overline{\text{CE}}$ high. In standby mode, all outputs are in a high impedance state, independent of $\overline{\text{OE}}/\text{VPP}$.

Two-line Output Control

Since EPROMs are often used in large memory arrays, the W27C512 provides two control inputs for multiple memory connections. Two-line control provides for lowest possible memory power dissipation and ensures that data bus contention will not occur.

System Considerations

An EPROM's power switching characteristics require careful device decoupling. System designers are interested in three supply current issues: standby current levels (I_{SB}), active current levels (I_{CC}), and transient current peaks produced by the falling and rising edges of $\overline{\text{CE}}$. Transient current magnitudes depend on the device output's capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between its VCC and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every eight devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection between VCC and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

TABLE OF OPERATING MODES

($\text{V}_{\text{PP}} = 12\text{V}$, $\text{V}_{\text{PE}} = 14\text{V}$, $\text{V}_{\text{HH}} = 12\text{V}$, $\text{V}_{\text{CP}} = 5\text{V}$, $\text{V}_{\text{CE}} = 5\text{V}$, $\text{X} = \text{V}_{\text{IH}}$ or V_{IL})

MODE	PINS					
	$\overline{\text{CE}}$	$\overline{\text{OE}}/\text{VPP}$	A0	A9	Vcc	OUTPUTS
Read	VIL	VIL	X	X	VCC	DOUT
Output Disable	VIL	VIH	X	X	VCC	High Z
Standby (TTL)	VIH	X	X	X	VCC	High Z
Standby (CMOS)	$\text{VCC} \pm 0.3\text{V}$	X	X	X	VCC	High Z
Program	VIL	VPP	X	X	VCP	DIN
Program Verify	VIL	VIL	X	X	VCC	DOUT
Program Inhibit	VIH	VPP	X	X	VCP	High Z
Erase	VIL	VPE	VIL	VPE	VCE	DIH
Erase Verify	VIL	VIL	X	X	3.75	DOUT
Erase Inhibit	VIH	VPE	X	X	VCE	High Z
Product Identifier-manufacturer	VIL	VIL	VIL	VHH	VCC	DA (Hex)
Product Identifier-device	VIL	VIL	VIH	VHH	VCC	08 (Hex)



DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Operation Temperature	0 to +70	°C
Storage Temperature	-65 to +125	°C
Voltage on all Pins with Respect to Ground Except \overline{OE}/V_{PP} , A9 and VCC Pins	-0.5 to VCC +0.5	V
Voltage on \overline{OE}/V_{PP} Pin with Respect to Ground	-0.5 to +14.5	V
Voltage on A9 Pin with Respect to Ground	-0.5 to +14.5	V
Voltage VCC Pin with Respect to Ground	-0.5 to +7	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Erase Characteristics

($T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	ILI	$V_{IN} = V_{IL} \text{ or } V_{IH}$	-10	-	10	μA
VCC Erase Current	ICP	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{PE}$	-	-	30	mA
VPP Erase Current	IPP	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{PE}$	-	-	30	mA
Input Low Voltage	VIL	-	-0.3	-	0.8	V
Input High Voltage	VIH	-	2.4	-	5.5	V
Output Low Voltage (Verify)	VOL	$I_{OL} = 2.1\text{ mA}$	-	-	0.45	V
Output High Voltage (Verify)	VOH	$I_{OH} = -0.4\text{ mA}$	2.4	-	-	-
A9 Erase Voltage	VID	-	13.75	14	14.25	V
VPP Erase Voltage	VPE	-	13.75	14	14.25	V
VCC Supply Voltage (Erase)	VCE	-	4.75	5.0	5.25	V
VCC Supply Voltage (Erase Verify)	VCE	-	3.5	3.75	4.0	V

Note: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.



CAPACITANCE

(Vcc = 5V, TA = 25° C, f = 1 MHz)

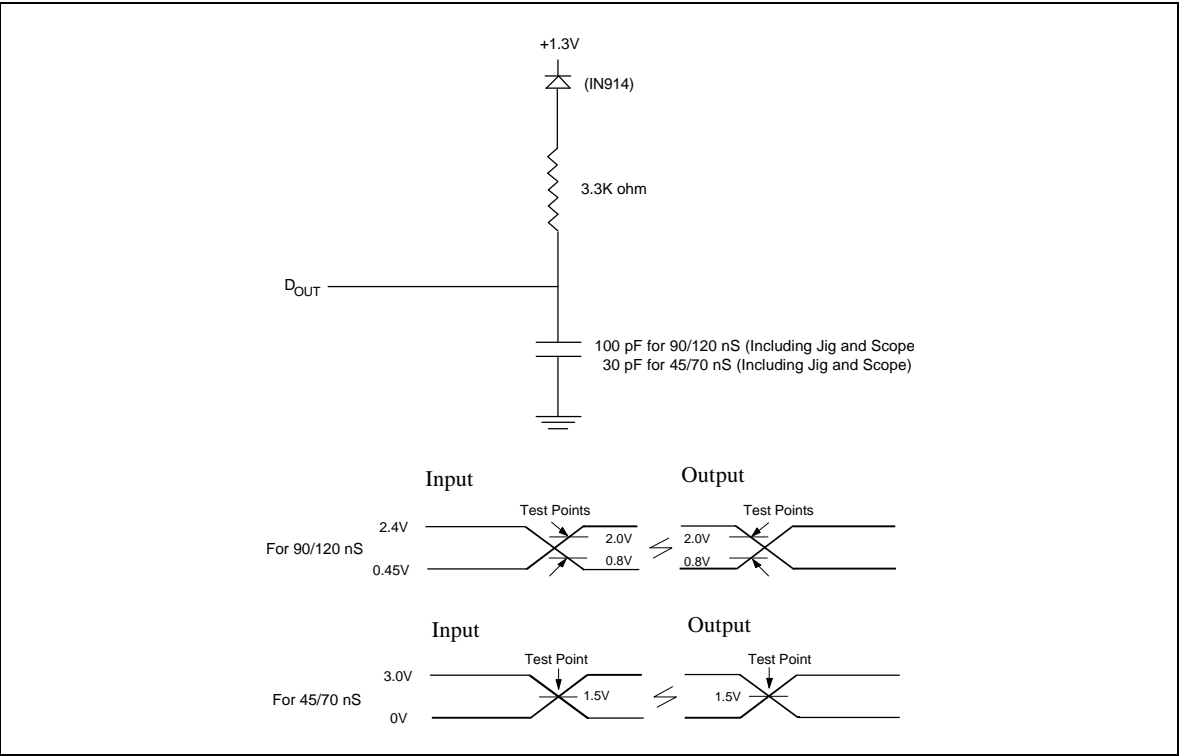
PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
Input Capacitance	CIN	VIN = 0V	6	pF
Output Capacitance	COUT	VOUT = 0V	12	pF

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS	
	45/70 nS	90/120 nS
Input Pulse Levels	0 to 3.0V	0.45V to 2.4V
Input Rise and Fall Times	5 nS	10 nS
Input and Output Timing Reference Level	1.5V/1.5V	0.8V/2.0V
Output Load	CL = 30 pF, IOH/IOL = -0.4 mA/2.1 mA	CL = 100 pF, IOH/IOL = -0.4 mA/2.1 mA

AC Test Load and Waveforms



READ OPERATION DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 70° C)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	ILI	V _{IN} = 0V to V _{CC}	-5	-	5	μA
Output Leakage Current	ILO	V _{OUT} = 0V to V _{CC}	-10	-	10	μA
Standby V _{CC} Current (TTL input)	ISB	$\overline{CE} = V_{IH}$	-	-	1.0	mA
Standby V _{CC} Current (CMOS input)	ISB1	$\overline{CE} = V_{CC} \pm 0.3V$	-	5	100	μA
V _{CC} Operating Current	ICC	$\overline{CE} = V_{IL}$ I _{OUT} = 0 mA, f = 5 MHz	-	-	30	mA
Input Low Voltage	V _{IL}	-	-0.3	-	0.8	V
Input High Voltage	V _{IH}	-	2.2	-	V _{CC} + 0.5	V
Output Low Voltage	V _{OL}	I _{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage	V _{OH}	I _{OH} = -0.4 mA	2.4	-	-	V

READ OPERATION AC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 70° C)

PARAMETER	SYM.	W27C512-45		W27C512-70		W27C512-90		W27C512-12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	TRC	45	-	70	-	90	-	120	-	nS
Chip Enable Access Time	TCE	-	45	-	70	-	90	-	120	nS
Address Access Time	TACC	-	45	-	70	-	90	-	120	nS
Output Enable Access Time	TOE	-	20	-	30	-	40	-	55	nS
\overline{OE} /V _{PP} High to High-Z Output	TDF	-	20	-	30	-	30	-	30	nS
Output Hold from Address Change	TOH	0	-	0	-	0	-	0	-	nS

Note: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

DC PROGRAMMING CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 25° C ±5° C)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	ILI	V _{IN} = V _{IL} or V _{IH}	-10	-	10	μA
V _{CC} Program Current	ICP	$\overline{CE} = V_{IL}$, $\overline{OE} /V_{PP} = V_{PP}$	-	-	30	mA
V _{PP} Program Current	IPP	$\overline{CE} = V_{IL}$, $\overline{OE} /V_{PP} = V_{PP}$	-	-	30	mA



DC Programming Characteristics, continued

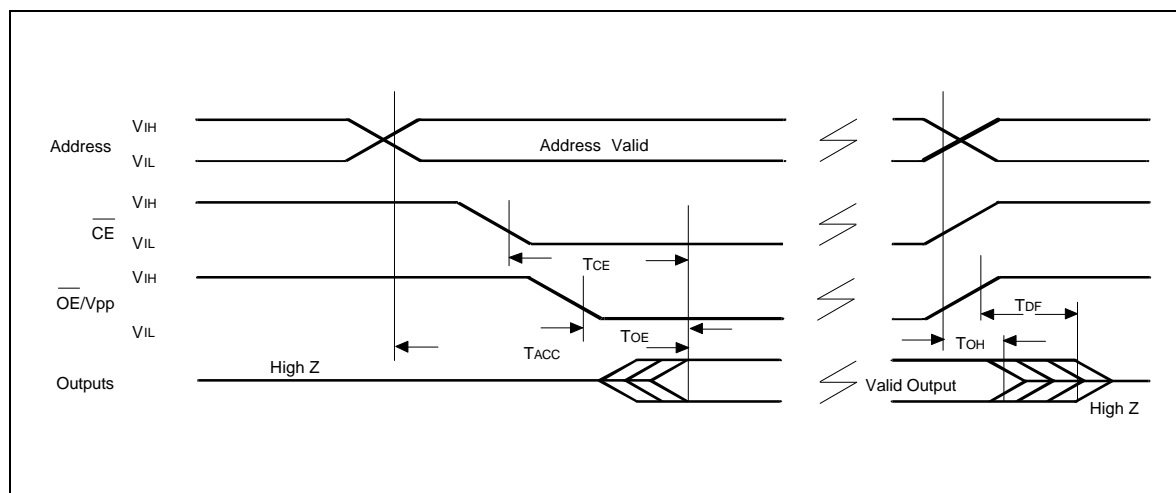
PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Low Voltage	V _{IL}	-	-0.3	-	0.8	V
Input High Voltage	V _{IH}	-	2.4	-	5.5	V
Output Low Voltage (Verify)	V _{OL}	I _{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage (Verify)	V _{OH}	I _{OH} = -0.4 mA	2.4	-	-	V
A9 Silicon I.D. Voltage	V _{ID}	-	11.5	12.0	12.5	V
V _{PP} Program Voltage	V _{PP}	-	11.75	12.0	12.25	V
V _{CC} Supply Voltage (Program)	V _{CP}	-	4.75	5.0	5.25	V

AC PROGRAMMING/ERASE CHARACTERISTICS(V_{CC} = 5.0V ±5%, T_A = 25° C ±5° C)

PARAMETER	SYM.	LIMITS			UNIT
		MIN.	TYP.	MAX.	
$\overline{\text{OE}}$ /V _{PP} Pulse Rise Time	TPRT	50	-	-	nS
Data Setup Time	TDS	2.0	-	-	μS
$\overline{\text{CE}}$ Program Pulse Width	TPWP	95	100	105	μS
$\overline{\text{CE}}$ Erase Pulse Width	TPWE	95	100	105	mS
Data Hold Time	TDH	2.0	-	-	μS
$\overline{\text{OE}}$ /V _{PP} Setup Time	TOES	2.0	-	-	μS
$\overline{\text{OE}}$ /V _{PP} Hold Time	TOEH	2.0	-	-	μS
Data Valid from $\overline{\text{CE}}$	TDV1	25	-	1	μS
Data Valid from Address Change	TDV2	25	-	1	μS
$\overline{\text{CE}}$ High to Output High Z	TDFP	0	-	130	nS
Address Setup Time	TAS	2.0	-	-	μS
Address Hold Time	TAH	0	-	-	μS
Address Hold Time after $\overline{\text{CE}}$ High (Erase)	TAHC	2.0	-	-	μS
$\overline{\text{OE}}$ /V _{PP} Valid after $\overline{\text{CE}}$ High	TVS	2.0	-	-	μS
$\overline{\text{OE}}$ /V _{PP} Recovery Time	TVR	2.0	-	-	μS
Address Access Time During Erase Verify (V _{CC} = 3.75V)	TACV	-	-	250	nS
Output Enable Access Time during Erase Verify (V _{CC} = 3.75V)	TOEV	-	-	150	nS

Note: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

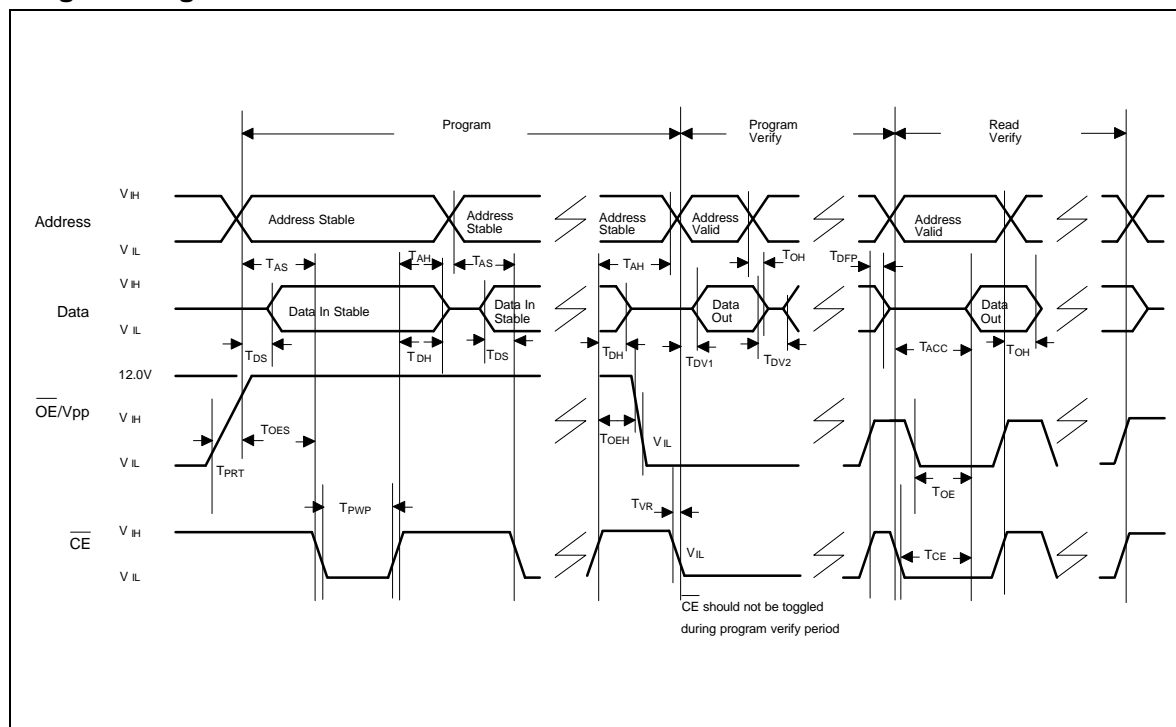
AC Read Waveform



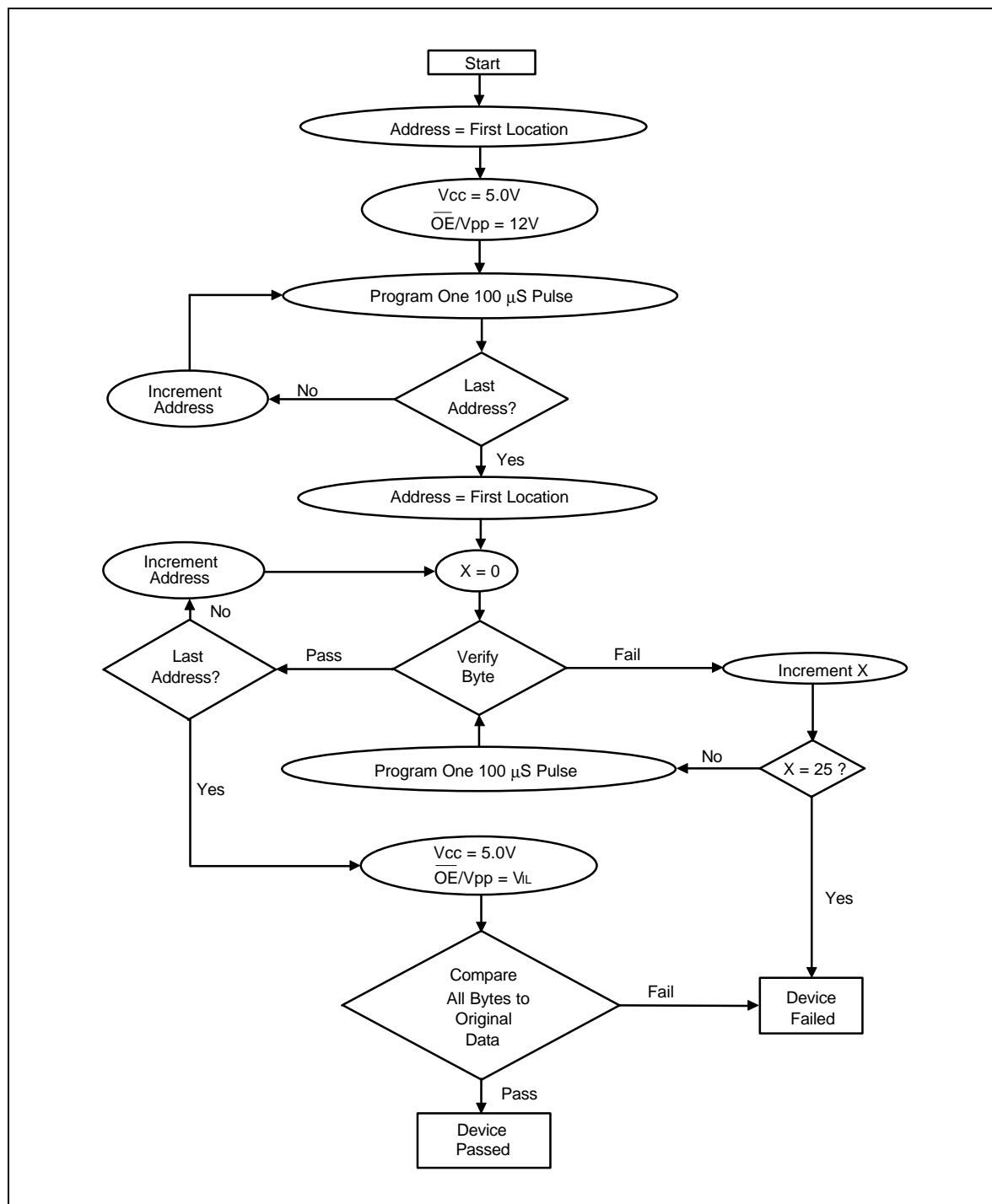
The timing diagram illustrates the sequence of operations for the 28C64 EPROM. It shows the relationship between the Address bus, Data bus, Vcc, OE/Vpp, and CE signals over time. Key operations include reading the company and device SIDs, performing a chip erase, verifying the erase, and performing a blank check read. The diagram specifies the required setup and hold times for each operation, ensuring reliable data transfer and successful programming/erasing.

Timing Waveforms, continued

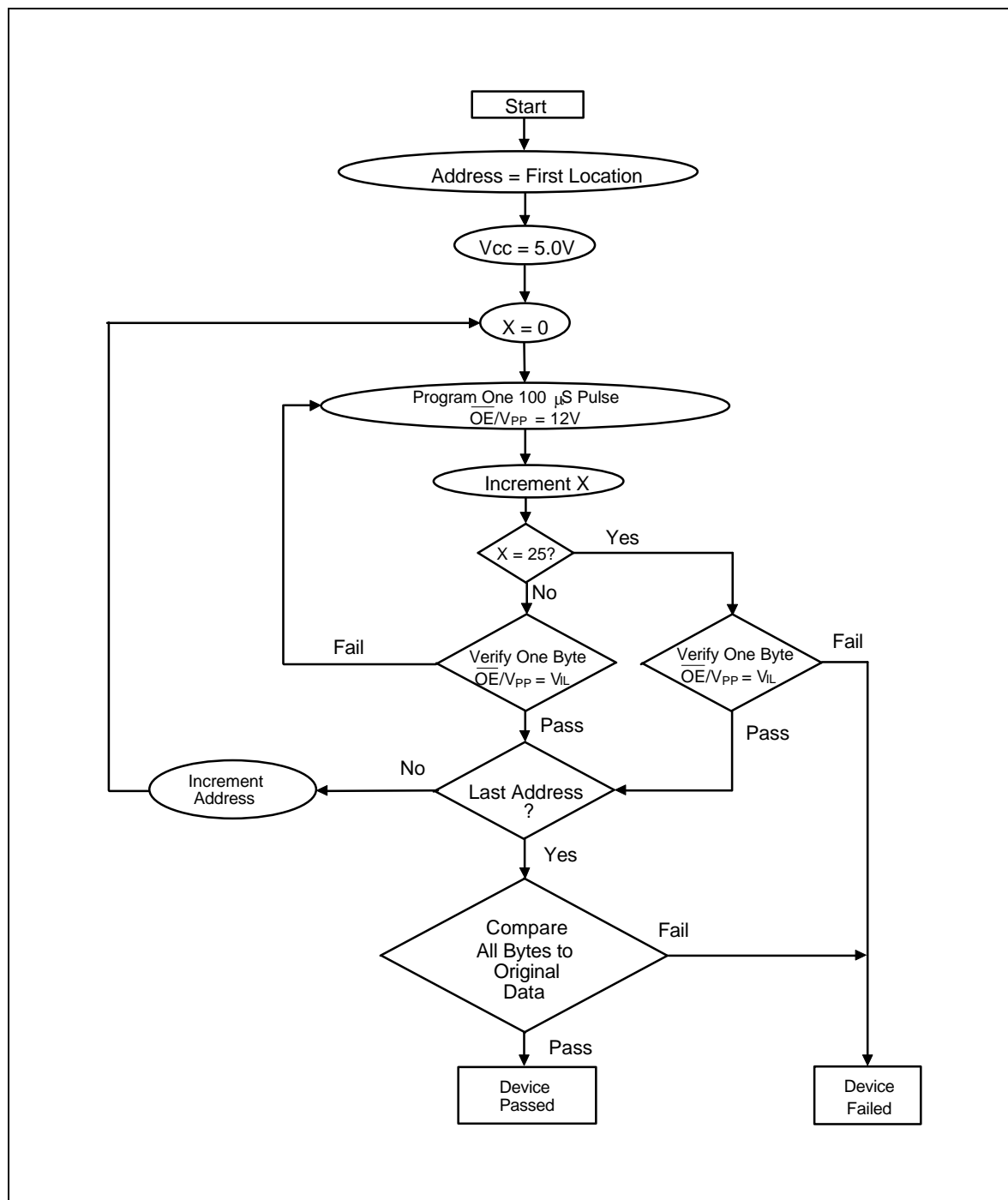
Programming Waveform



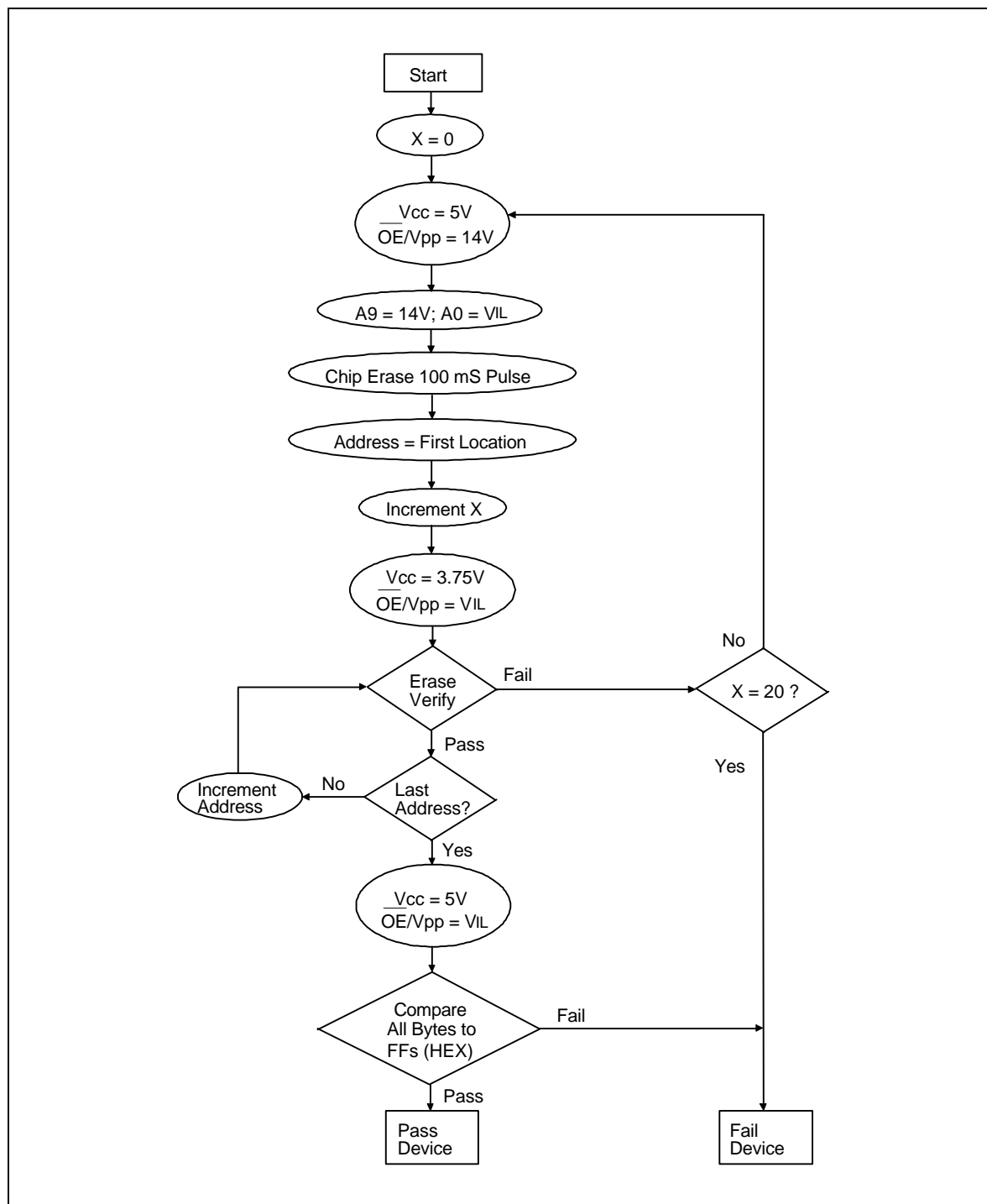
SMART PROGRAMMING ALGORITHM 1



SMART PROGRAMMING ALGORITHM 2



SMART ERASE ALGORITHM



W27C512



ORDERING INFORMATION

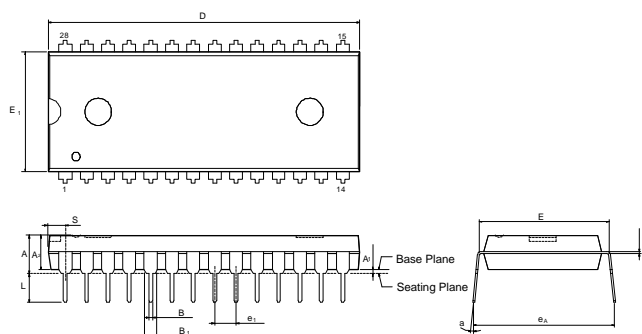
PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W27C512-45	45	30	100	600 mil DIP
W27C512-70	70	30	100	600 mil DIP
W27C512-90	90	30	100	600 mil DIP
W27C512-12	120	30	100	600 mil DIP
W27C512P-45	45	30	100	32-pin PLCC
W27C512P-70	70	30	100	32-pin PLCC
W27C512P-90	90	30	100	32-pin PLCC
W27C512P-12	120	30	100	32-pin PLCC

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

28-pin P-DIP

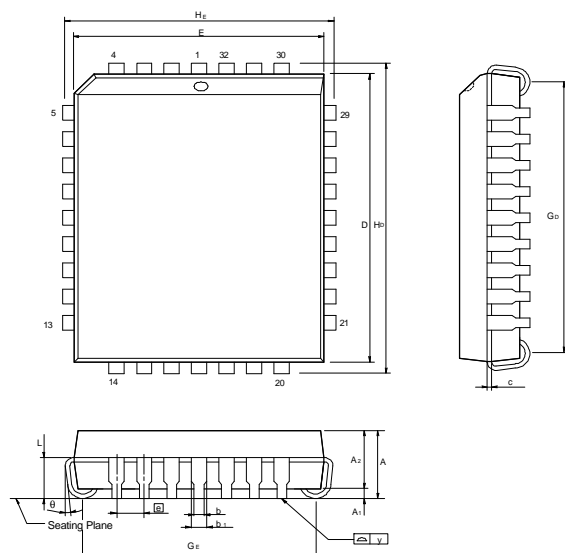


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A ₁	0.010	—	—	0.25	—	—
A ₂	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B ₁	0.058	0.060	0.064	1.47	1.52	1.63
C	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.460	1.470	—	37.08	37.34
E	0.590	0.600	0.610	14.99	15.24	15.49
E ₁	0.540	0.545	0.550	13.72	13.84	13.97
e ₁	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e _A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.090	—	—	2.29

Notes:

1. Dimensions D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimensions D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

32-pin PLCC



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.140	—	—	3.56
A ₁	0.020	—	—	0.50	—	—
A ₂	0.105	0.110	0.115	2.67	2.80	2.93
b ₁	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
E ₁	0.044	0.050	0.056	1.12	1.27	1.42
G ₂	0.490	0.510	0.530	12.45	12.95	13.46
G ₁	0.390	0.410	0.430	9.91	10.41	10.92
H ₂	0.585	0.590	0.595	14.86	14.99	15.11
H ₁	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches.
4. General appearance spec. should be based on final visual inspection spec.



VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Mar. 1998		Initial Issued
A2	Sep. 1998	6	Correct Input High Voltage (VIH) from 2.0 (min) to 2.2 (max)
		4 , 6	Correct VCC from 5.0 \pm 10% to 5.0 \pm 5%
A3	Aug. 1999	1, 5, 6, 13	Add 45 nS binning
		2, 3	Modify function description (VIL and VIH): VIL \rightarrow Low; VIH \rightarrow High
A4	Nov. 1999	6	Typo correction



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Note: All data and specifications are subject to change without notice.

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