

19-0099; Rev 2; 9/95

# MAXIM

## +3V Voltage Monitoring, Low-Cost, $\mu$ P Supervisory Circuits

### General Description

The MAX706P/R/S/T and MAX708R/S/T microprocessor ( $\mu$ P) supervisory circuits reduce the complexity and number of components required to monitor +3V power-supply levels in +3V to +5V  $\mu$ P systems. These devices significantly improve system reliability and accuracy compared to separate ICs or discrete components.

The MAX706P/R/S/T supervisory circuits provide the following four functions:

- 1) A reset output during power-up, power-down, and brownout conditions.
- 2) An independent watchdog output that goes low if the watchdog input has not been toggled within 1.6sec.
- 3) A 1.25V threshold detector for power-fail warning, low-battery detection, or for monitoring a power supply other than the main supply.
- 4) An active-low manual-reset input.

The only difference between the MAX706R, MAX706S, and MAX706T is the reset-threshold voltage levels, which are 2.63V, 2.93V, and 3.08V, respectively. All have active-low reset output signals. The MAX706P is identical to the MAX706R, except its reset output signal is active-high.

The MAX708R/S/T provide the same functions as the MAX706R/S/T, except they do not have a watchdog timer. Instead, they provide both  $\overline{\text{RESET}}$  and RESET outputs. As with the MAX706, devices with R, S, and T suffixes have reset thresholds of 2.63V, 2.93V and 3.08V, respectively.

All seven devices are offered in 8-pin SO, DIP, and  $\mu$ MAX packages.

### Features

- ◆  $\mu$ MAX Package: Smallest 8-Pin SO
- ◆ Precision Supply-Voltage Monitor  
2.63V (MAX706P/R, MAX708R)  
2.93V (MAX706S, MAX708S)  
3.08V (MAX706T, MAX708T)
- ◆ 200ms Reset Time Delay
- ◆ Debounced TTL/CMOS-Compatible Manual-Reset Input
- ◆ 100 $\mu$ A Quiescent Current
- ◆ Watchdog Timer (MAX706P/R/S/T only):  
1.6sec Timeout
- ◆ Reset Output Signal:  
Active-High Only (MAX706P)  
Active-Low Only (MAX706R/S/T)  
Active-High and Active-Low (MAX708R/S/T)
- ◆ Voltage Monitor for Power-Fail or Low-Battery Warning
- ◆ 8-Pin Surface-Mount Package
- ◆ Guaranteed  $\overline{\text{RESET}}$  Assertion to VCC = 1V

### Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX706PCPA	0°C to +70°C	8 Plastic DIP
MAX706PCSA	0°C to +70°C	8 SO
MAX706PCUA	0°C to +70°C	8 $\mu$ MAX
MAX706PEPA	-40°C to +85°C	8 Plastic DIP
MAX706PESA	-40°C to +85°C	8 SO
MAX706PMJA	-55°C to +125°C	8 CERDIP*

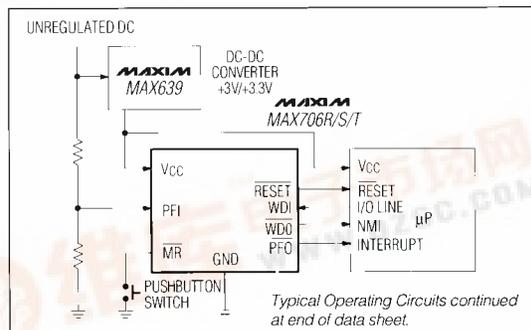
Ordering Information continued at end of data sheet.

\* Contact factory for availability and processing to MIL-STD-883.

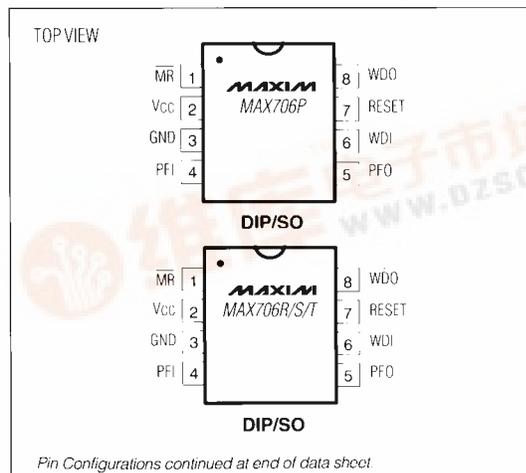
### Applications

Battery-Powered Equipment  
Portable Instruments  
Computers  
Controllers  
Intelligent Instruments  
Critical  $\mu$ P Power Monitoring

### Typical Operating Circuits



### Pin Configurations



MAX706P/R/S/T, MAX708R/S/T

MAXIM

Maxim Integrated Products 1

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### ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)		$\mu$ MAX (derate 4.1mW/°C above +70°C).....	330mW
V <sub>CC</sub> .....	-0.3V to 6.0V	CERDIP (derate 8.00mW/°C above +70°C).....	640mW
All Other Inputs (Note 1).....	-0.3V to (V <sub>CC</sub> + 0.3V)	Operating Temperature Ranges:	
Input Current		MAX70_C_.....	0°C to +70°C
V <sub>CC</sub> .....	20mA	MAX70_E_.....	-40°C to +85°C
GND.....	20mA	MAX70_M_.....	-55°C to +125°C
Output Current (all outputs).....	20mA	Storage Temperature Range.....	-65°C to +160°C
Continuous Power Dissipation		Lead Temperature (soldering, 10sec).....	+300°C
Plastic DIP (derate 9.09mW/°C above +70°C).....	727mW		
SO (derate 5.88mW/°C above +70°C).....	471mW		

**Note 1:** The input voltage limits on PFI, WDI and  $\overline{MR}$  can be exceeded if the input current is less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS

(MAX70\_P/R: V<sub>CC</sub> = 2.70V to 5.5V, MAX70\_S: V<sub>CC</sub> = 3.00V to 5.5V, MAX70\_T: V<sub>CC</sub> = 3.15V to 5.5V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V <sub>CC</sub>	MAX70_C	1.0		5.5	V
		MAX70_E/M	1.2		5.5	
Supply Current	I <sub>SUPPLY</sub>	V <sub>CC</sub> < 3.6V	MAX706_C	90	200	$\mu$ A
			MAX706_E/M	90	300	
			MAX708_C	50	200	
			MAX708_E/M	50	300	
		V <sub>CC</sub> < 5.5V	MAX706_C	135	350	
			MAX706_E/M	135	500	
			MAX708_C	65	350	
			MAX708_E/M	65	500	
Reset Threshold (Note 2)	V <sub>RST</sub>	MAX70_P/R	2.55	2.63	2.70	V
		MAX70_S	2.85	2.93	3.00	
		MAX70_T	3.00	3.08	3.15	
Reset Threshold Hysteresis (Note 2)			20			mV
Reset Pulse Width (Note 2)	t <sub>RST</sub>	MAX70_P/R: V <sub>CC</sub> = 3.0V; MAX70_S/T: V <sub>CC</sub> = 3.3V	140	200	280	ms
		V <sub>CC</sub> = 5.0V		200		
RESET Output Voltage (MAX70_R/S/T)	V <sub>OH</sub>	V <sub>RST</sub> (max) < V <sub>CC</sub> < 3.6V	I <sub>SOURCE</sub> = 500 $\mu$ A	0.8 x V <sub>CC</sub>		V
	V <sub>OL</sub>		I <sub>SINK</sub> = 1.2mA	0.3		
	V <sub>OH</sub>	4.5V < V <sub>CC</sub> < 5.5V	I <sub>SOURCE</sub> = 800 $\mu$ A	V <sub>CC</sub> - 1.5		
	V <sub>OL</sub>		I <sub>SINK</sub> = 3.2mA	0.4		
	V <sub>OL</sub>	MAX70_C: V <sub>CC</sub> = 1.0V, I <sub>SINK</sub> = 50 $\mu$ A	0.3			
		MAX70_E/M: V <sub>CC</sub> = 1.2V, I <sub>SINK</sub> = 100 $\mu$ A	0.3			
RESET Output Voltage (MAX706P)	V <sub>OH</sub>	V <sub>RST</sub> (max) < V <sub>CC</sub> < 3.6V	I <sub>SOURCE</sub> = 215 $\mu$ A	V <sub>CC</sub> - 0.6		V
	V <sub>OL</sub>		I <sub>SINK</sub> = 1.2mA	0.3		
	V <sub>OH</sub>	4.5V < V <sub>CC</sub> < 5.5V	I <sub>SOURCE</sub> = 800 $\mu$ A	V <sub>CC</sub> - 1.5		
	V <sub>OL</sub>		I <sub>SINK</sub> = 3.2mA	0.4		

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### ELECTRICAL CHARACTERISTICS (continued)

(MAX70\_P/R:  $V_{CC} = 2.70V$  to  $5.5V$ , MAX70\_S:  $V_{CC} = 3.00V$  to  $5.5V$ , MAX70\_T:  $V_{CC} = 3.15V$  to  $5.5V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RESET Output Voltage (MAX708_)	$V_{OH}$	$V_{RST}(\max) < V_{CC} < 3.6V$	$I_{SOURCE} = 500\mu A$	$0.8 \times V_{CC}$		0.3	V
	$V_{OL}$		$I_{SINK} = 500\mu A$				
	$V_{OH}$	$4.5V < V_{CC} < 5.5V$	$I_{SOURCE} = 800\mu A$	$V_{CC} - 1.5$		0.4	
	$V_{OL}$		$I_{SINK} = 1.2mA$				
Watchdog Timeout Period (MAX706_)	$t_{WD}$	MAX70_P/R: $V_{CC} = 3.0V$ ; MAX70_S/T: $V_{CC} = 3.3V$		1.0	1.6	2.25	sec
WDI Pulse Width (MAX706_)	$t_{WP}$	$V_{IL} = 0.4V$ ; $V_{IH} = 0.8 \times V_{CC}$	$V_{RST}(\max) < V_{CC} < 3.6V$	100			ns
			$4.5V < V_{CC} < 5.5V$	50			
WDI Input Threshold (MAX706_)	$V_{IL}$	$V_{RST}(\max) < V_{CC} < 3.6V$	Low			0.6	V
	$V_{IH}$		High	$0.7 \times V_{CC}$			
	$V_{IL}$	$V_{CC} = 5.0V$	Low			0.8	
	$V_{IH}$		High	3.5			
WDI Input Current (MAX706_)		$WDI = 0V$ or $V_{CC}$		-1.0	0.02	1.0	$\mu A$
WDO Output Voltage (MAX706_)	$V_{OH}$	$V_{RST}(\max) < V_{CC} < 3.6V$	$I_{SOURCE} = 500\mu A$	$0.8 \times V_{CC}$		0.3	V
	$V_{OL}$		$I_{SINK} = 500\mu A$				
	$V_{OH}$	$4.5V < V_{CC} < 5.5V$	$I_{SOURCE} = 800\mu A$	$V_{CC} - 1.5$		0.4	
	$V_{OL}$		$I_{SINK} = 1.2mA$				
MR Pull-Up Current		$MR = 0V$	$V_{RST}(\max) < V_{CC} < 3.6V$	25	70	250	$\mu A$
			$4.5V < V_{CC} < 5.5V$	100	250	600	
MR Pulse Width	$t_{MR}$	$V_{RST}(\max) < V_{CC} < 3.6V$ ; $4.5V < V_{CC} < 5.5V$		500			ns
				150			
MR Input Threshold	$V_{IL}$	$V_{RST}(\max) < V_{CC} < 3.6V$	Low			0.6	V
	$V_{IH}$		High	$0.7 \times V_{CC}$			
	$V_{IL}$	$4.5V < V_{CC} < 5.5V$	Low			0.8	
	$V_{IH}$		High	2.0			
MR to Reset Out Delay (Note 2)	$t_{MD}$	$V_{RST}(\max) < V_{CC} < 3.6V$ ; $4.5V < V_{CC} < 5.5V$				750	ns
						250	
PFI Input Threshold		MAX70_P/R: $V_{CC} = 3.0V$ ; MAX70_S/T: $V_{CC} = 3.3V$ , PFI falling		1.20	1.25	1.30	V
PFI Input Current				-25	0.01	25	nA
PFO Output Voltage	$V_{OH}$	$V_{RST}(\max) < V_{CC} < 3.6V$	$I_{SOURCE} = 500\mu A$	$0.8 \times V_{CC}$		0.3	V
	$V_{OL}$		$I_{SINK} = 1.2mA$				
	$V_{OH}$	$4.5V < V_{CC} < 5.5V$	$I_{SOURCE} = 800\mu A$	$V_{CC} - 1.5$		0.4	
	$V_{OL}$		$I_{SINK} = 3.2mA$				

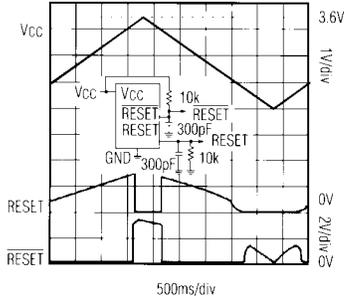
**Note 2:** Applies to both RESET in the MAX70\_R/S/T, and RESET in the MAX706P and MAX708R/S/T.

**MAX706P/R/S/T, MAX708R/S/T**

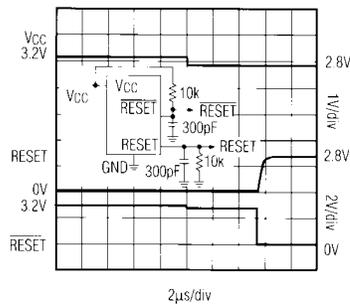
## **+3V Voltage Monitoring, Low-Cost, $\mu$ P Supervisory Circuits**

### **Typical Operating Characteristics**

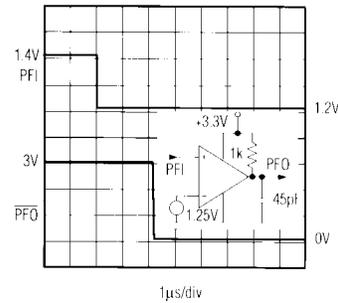
**RESET,  $\overline{\text{RESET}}$  OUTPUT VOLTAGES  
vs. SUPPLY VOLTAGE  
(RESET OUTPUTS AND RESET THRESHOLDS  
SHOWN FOR MAX708T,  $T_A = +25^\circ\text{C}$ )**



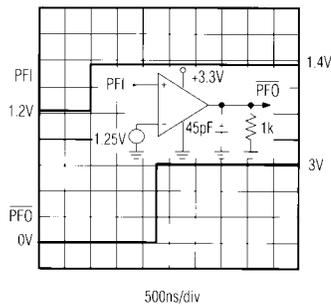
**RESET,  $\overline{\text{RESET}}$  RESPONSE TIMES**



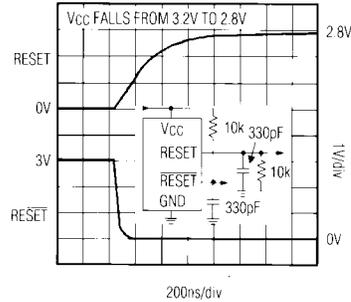
**POWER-FAIL COMPARATOR  
ASSERTION RESPONSE TIME**



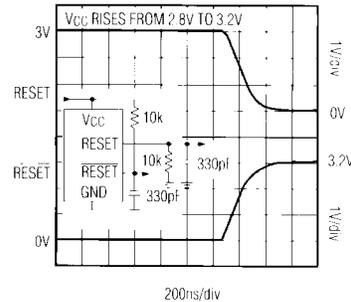
**POWER-FAIL COMPARATOR  
DEASSERTION RESPONSE TIME**



**RESET,  $\overline{\text{RESET}}$   
RISE AND FALL TIMES  
(RESET ASSERTED)**



**RESET,  $\overline{\text{RESET}}$   
RISE AND FALL TIMES  
(RESET DEASSERTED)**



## +3V Voltage Monitoring, Low-Cost, $\mu$ P Supervisory Circuits

### Pin Description

PIN						NAME	FUNCTION
MAX706P		MAX706R/S/T		MAX708R/S/T			
DIP/SO	$\mu$ MAX	DIP/SO	$\mu$ MAX	DIP/SO	$\mu$ MAX		
1	3	1	3	1	3	$\overline{\text{MR}}$	Manual-Reset Input. When pulled below 0.6V, $\overline{\text{MR}}$ triggers a reset pulse. It is TTL/CMOS-compatible when $V_{CC} = 5V$ and can be shorted to ground with a switch. This active-low input has an internal 70 $\mu$ A pull-up current. Leave floating or connect to $V_{CC}$ if not used.
2	4	2	4	2	4	$V_{CC}$	Supply-Voltage Input
3	5	3	5	3	5	GND	Ground
4	6	4	6	4	6	PFI	Power-Fail Comparator Input. When PFI is less than 1.25V, PFO goes low; otherwise PFO remains high. Connect PFI to GND when not used.
5	7	5	7	5	7	$\overline{\text{PFO}}$	Power-Fail Output. When PFI is less than 1.25V, $\overline{\text{PFO}}$ goes low and sinks current; otherwise, $\overline{\text{PFO}}$ remains high. Leave unconnected if not used.
6	8	6	8	-	-	WDI	Watchdog Input. A rising or falling edge must occur at WDI within 1.6sec or $\overline{\text{WDO}}$ goes low (Figure 4). The internal watchdog timer is reset to zero when reset is asserted or when a transition occurs at WDI. The watchdog function cannot be disabled.
-	-	-	-	6	8	N.C.	No Connect—not internally connected.
-	-	7	1	7	1	$\overline{\text{RESET}}$	Active-Low Reset Output. $\overline{\text{RESET}}$ remains low while $V_{CC}$ is below the reset threshold or $\overline{\text{MR}}$ is held low. It remains low for 200ms after the reset condition are terminated (Figure 3).
7	1	-	-	8	2	RESET	Active-High Reset Output. RESET remains high while $V_{CC}$ is below the reset threshold or $\overline{\text{MR}}$ is held low. It remains high for 200ms after the reset conditions are terminated (Figure 3).
8	2	8	2	-	-	$\overline{\text{WDO}}$	Watchdog Output. $\overline{\text{WDO}}$ goes low when a transition does not occur at WDI within 1.6sec, and remains low until a transition occurs at WDI (indicating the watchdog interrupt has been serviced). $\overline{\text{WDO}}$ also goes low when $V_{CC}$ falls below the reset threshold; however, unlike the reset output signal, $\overline{\text{WDO}}$ goes high as soon as $V_{CC}$ exceeds the reset threshold.

MAX706P/R/S/T, MAX708R/S/T

### Detailed Description

#### $\overline{\text{RESET}}$ and RESET Outputs

A microprocessor's ( $\mu$ P's) reset input starts it in a known state. When the  $\mu$ P is in an unknown state, it should be held in reset. The MAX706P/R/S/T and MAX708R/S/T assert reset when  $V_{CC}$  is low, preventing code execution errors during power-up, power-down or brownout conditions.

On power-up, once  $V_{CC}$  reaches 1V,  $\overline{\text{RESET}}$  is guaranteed to be a logic low and RESET is guaranteed to be a logic high. As  $V_{CC}$  rises,  $\overline{\text{RESET}}$  and RESET remain asserted. Once  $V_{CC}$  exceeds the reset threshold, the internal timer causes  $\overline{\text{RESET}}$  and RESET to be deasserted after a time equal to the reset pulse width, which is typically 200ms (Figure 3). If a power-fail or brownout condition occurs (i.e.  $V_{CC}$  drops below the reset threshold),  $\overline{\text{RESET}}$  and RESET are asserted. As long as  $V_{CC}$  remains below the reset threshold, the internal timer is continually reset, causing the  $\overline{\text{RESET}}$  and RESET outputs

to remain asserted. Thus, a brownout condition that interrupts a previously initiated reset pulse causes an additional 200ms delay from the time the latest interruption occurred. On power-down, once  $V_{CC}$  drops below the reset threshold,  $\overline{\text{RESET}}$  and RESET are guaranteed to be asserted for  $V_{CC} \geq 1V$ .

The MAX706P provides a RESET signal, the MAX706R/S/T provide a  $\overline{\text{RESET}}$  signal, and the MAX708R/S/T provide both  $\overline{\text{RESET}}$  and RESET.

#### Watchdog Timer (MAX706P/R/S/T)

The MAX706P/R/S/T watchdog circuit monitors the  $\mu$ P's activity. If the  $\mu$ P does not toggle the Watchdog Input (WDI) within 1.6sec, the Watchdog Output ( $\overline{\text{WDO}}$ ) goes low (Figure 4). If the reset signal is asserted, the watchdog timer will be reset to zero and disabled. As soon as reset is released, the timer starts counting. WDI can detect pulses as narrow as 100ns with a 2.7V supply and 50ns with a 4.5V supply.

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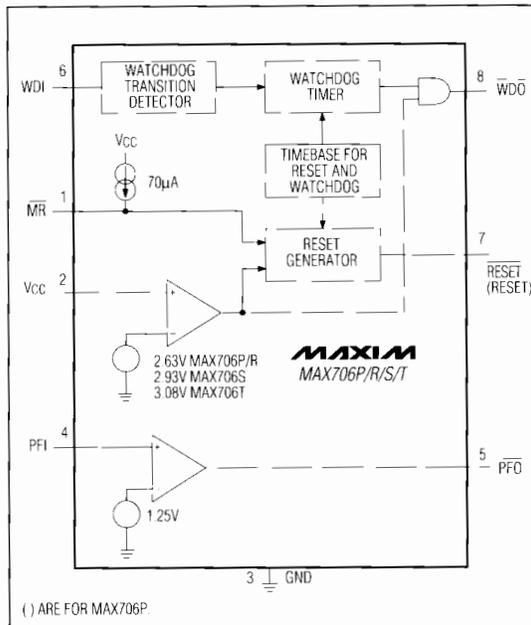


Figure 1. MAX706P/R/S/T Block Diagram

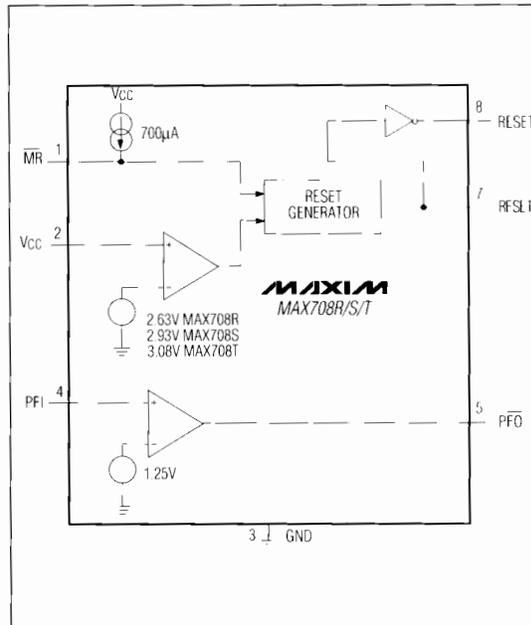


Figure 2. MAX708R/S/T Block Diagram

$\overline{WDO}$  can be connected to the non-maskable interrupt (NMI) input of a  $\mu$ P. When  $V_{CC}$  drops below the reset threshold,  $\overline{WDO}$  immediately goes low, even if the watchdog timer has not timed out (Figure 3). Normally, this would trigger an NMI, but since reset is asserted simultaneously, the NMI is overridden.  $\overline{WDO}$  can instead be connected to  $\overline{MR}$  to generate a reset pulse when the watchdog times out.

### Manual Reset

The Manual-Reset ( $\overline{MR}$ ) input allows  $\overline{RESET}$  and  $RESET$  to be activated by a pushbutton switch. The switch is effectively debounced by the 140ms minimum reset pulse width.  $\overline{MR}$  can be driven by an external logic line since it is TTL/CMOS compatible. The minimum  $\overline{MR}$  input pulse width is 500ns when  $V_{CC} = +3V$  and 150ns when  $V_{CC} = +5V$ . Leave  $\overline{MR}$  floating or tie to  $V_{CC}$  when not used.

### Power-Fail Comparator

The power-fail comparator can be used for various purposes because its output and noninverting input are not internally connected. The inverting input is internally connected to a 1.25V reference. The power-fail com-

parator has 10mV of hysteresis which prevents repeated triggering of the Power-Fail Output ( $\overline{PFO}$ ).

To build an early-warning power-failure circuit, use the Power-Fail Comparator Input (PFI) to monitor the unregulated DC supply voltage (see *Typical Operating Circuit*). Connect the PFI pin to a resistor-divider network such that the voltage at PFI falls below 1.25V just before the regulator drops out. Use  $\overline{PFO}$  to interrupt the  $\mu$ P so it can prepare for an orderly power-down.

Regulated and unregulated voltages can be monitored by simply adjusting the PFI resistor-divider network values to the appropriate ratio. In addition, the reset signal can be asserted at voltages other than the  $V_{CC}$  reset threshold, as shown in Figure 5. Connect  $\overline{PFO}$  to  $\overline{MR}$  to initiate a reset pulse when the 12V supply drops below a user-specified threshold (11V in this example) or when  $V_{CC}$  falls below the reset threshold.

## Applications Information

### Operation with +3V and +5V Supplies

The MAX706P/R/S/T and MAX708R/S/T provide voltage monitoring at the reset threshold (2.63V to 3.08V) when powered from either +3V or +5V. They are ideal in porta-

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**MAX706P/R/S/T, MAX708R/S/T**

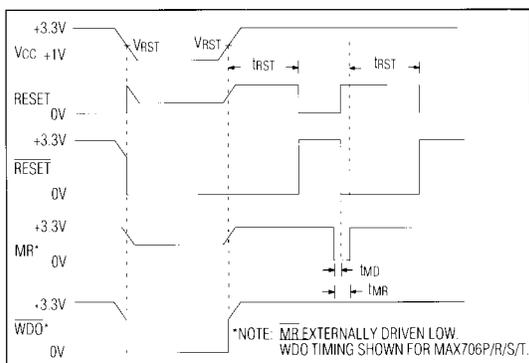


Figure 3. RESET, RESET, MR and WDO Timing

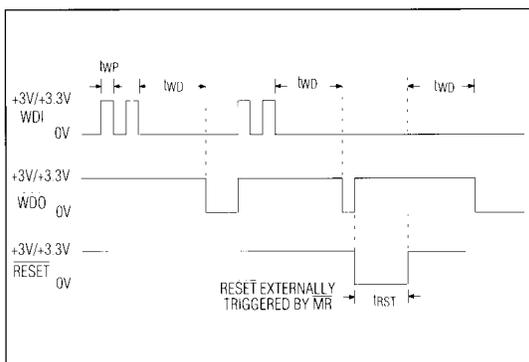


Figure 4. MAX706P/R/S/T Watchdog Timing

ble-instrument applications where power can be supplied from either a +3V battery or an AC-DC wall adapter that generates +5V (a +5V supply allows a  $\mu$ P or microcontroller to run faster than a +3V supply). With a +3V supply, these ICs consume less power, but output drive capability is reduced, the MR-to-RESET delay time increases, and the MR minimum pulse width increases. The *Electrical Characteristics* table provides specifications for operation with both +3V and +5V supplies.

### Ensuring a Valid RESET Output Down to $V_{CC} = 0V$

When  $V_{CC}$  falls below 1V, the MAX706R/S/T and MAX708R/S/T RESET output no longer sinks current; it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left as open circuits. If a pull-down resistor is added to the RESET pin, as shown in Figure 6, any stray charge or leakage currents will flow to ground, holding RESET low. Resistor

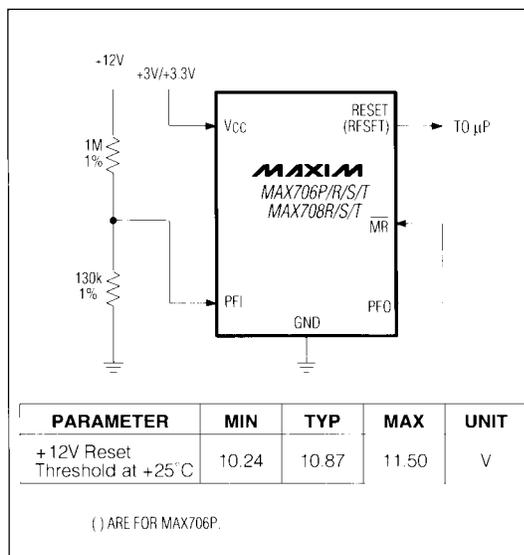


Figure 5. Monitoring Both +3V/+3.3V and +12V

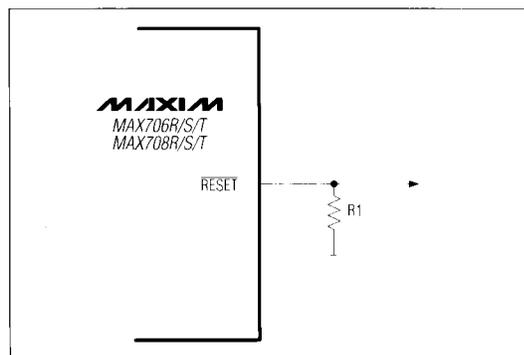


Figure 6. RESET Valid to Ground Circuit

value R1 is not critical, but it should not load RESET and should be small enough to pull RESET and the input it is driving to ground. 100k $\Omega$  is suggested for R1.

### Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of PFO when  $V_{IN}$  is near the power-fail comparator trip point. Figure 7 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 such that PFI sees 1.25V when  $V_{IN}$  falls to the desired trip point ( $V_{TRIP}$ ). Resistor R3 adds hysteresis. R3 will typically be an order of

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magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1 $\mu$ A to ensure that the 25nA max PFI input current does not shift the trip point significantly. R3 should be larger than 10k $\Omega$  to prevent it from loading down the PFO pin. Capacitor C1 adds noise rejection.

### Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using the circuit of Figure 8. When the negative supply is valid,  $\overline{\text{PFO}}$  is low. When the negative supply voltage drops,  $\overline{\text{PFO}}$  goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the VCC voltage, and resistors R1 and R2.

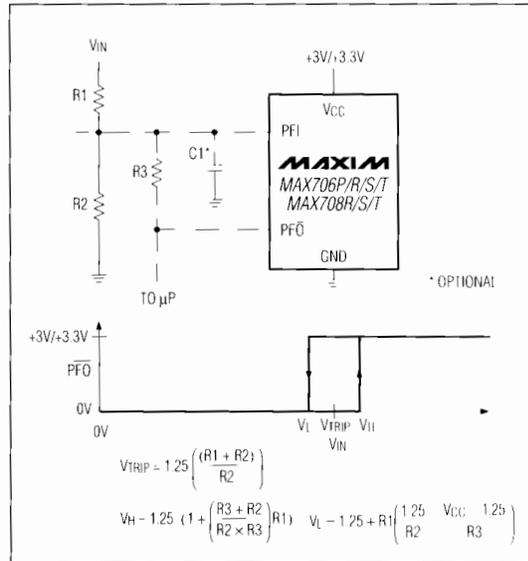


Figure 7. Adding Hysteresis to the Power-Fail Comparator

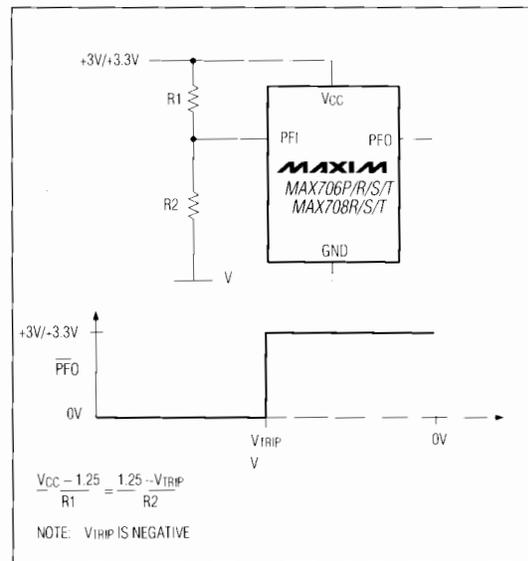
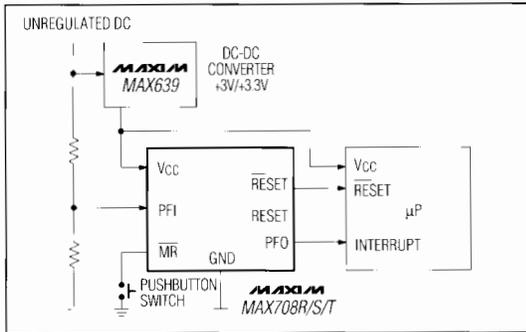


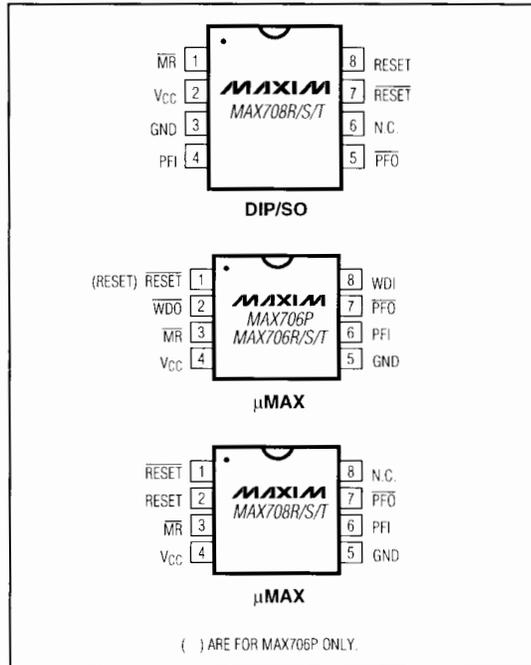
Figure 8. Monitoring a Negative Voltage

## +3V Voltage Monitoring, Low-Cost, $\mu$ P Supervisory Circuits

### Typical Operating Circuits (continued)



### Pin Configurations (continued)



**MAX706P/R/S/T, MAX708R/S/T**

### Chip Information

TRANSISTOR COUNT: 572

## +3V Voltage Monitoring, Low-Cost, $\mu$ P Supervisory Circuits

**MAX706P/R/S/T, MAX708R/S/T**

### Ordering Information (continued)

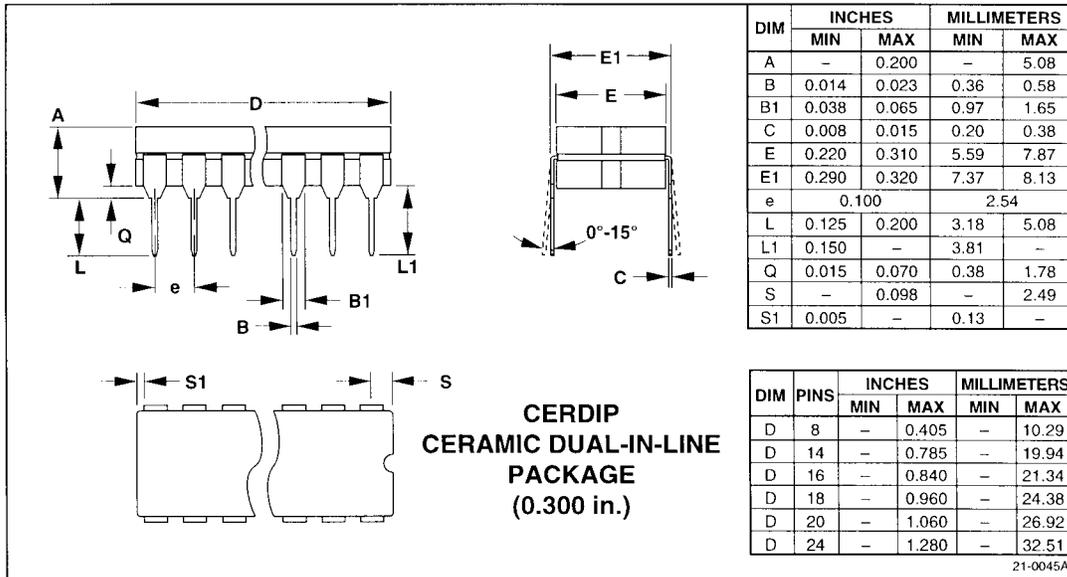
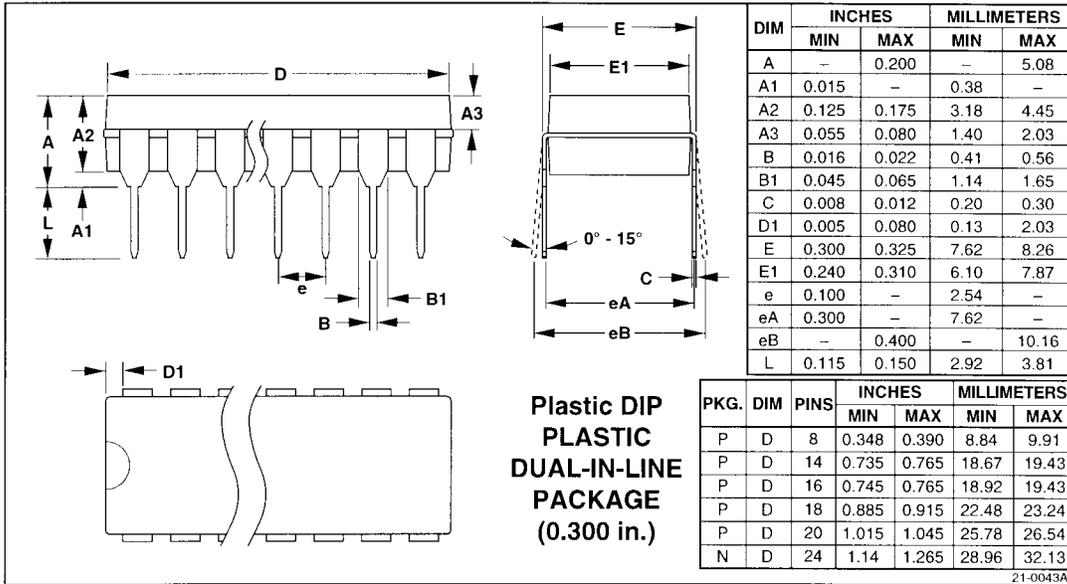
PART	TEMP. RANGE	PIN-PACKAGE
<b>MAX706R</b> CPA	0°C to +70°C	8 Plastic DIP
MAX706RCSA	0°C to +70°C	8 SO
MAX706RCUA	0°C to +70°C	8 $\mu$ MAX
MAX706REPA	-40°C to +85°C	8 Plastic DIP
MAX706RESA	-40°C to +85°C	8 SO
MAX706RMJA	-55°C to +125°C	8 CERDIP*
<b>MAX706S</b> CPA	0°C to +70°C	8 Plastic DIP
MAX706SCSA	0°C to +70°C	8 SO
MAX706SCUA	0°C to +70°C	8 $\mu$ MAX
MAX706SEPA	-40°C to +85°C	8 Plastic DIP
MAX706SESA	-40°C to +85°C	8 SO
MAX706SMJA	-55°C to +125°C	8 CERDIP*
<b>MAX706T</b> CPA	0°C to +70°C	8 Plastic DIP
MAX706TCSA	0°C to +70°C	8 SO
MAX706TCUA	0°C to +70°C	8 $\mu$ MAX
MAX706TEPA	-40°C to +85°C	8 Plastic DIP
MAX706TESA	-40°C to +85°C	8 SO
MAX706TMJA	-55°C to +125°C	8 CERDIP*
<b>MAX708R</b> CPA	0°C to +70°C	8 Plastic DIP
MAX708RCSA	0°C to +70°C	8 SO
MAX708RCUA	0°C to +70°C	8 $\mu$ MAX
MAX708REPA	-40°C to +85°C	8 Plastic DIP
MAX708RESA	-40°C to +85°C	8 SO
MAX708RMJA	-55°C to +125°C	8 CERDIP*
<b>MAX708S</b> CPA	0°C to +70°C	8 Plastic DIP
MAX708SCSA	0°C to +70°C	8 SO
MAX708SCUA	0°C to +70°C	8 $\mu$ MAX
MAX708SEPA	-40°C to +85°C	8 Plastic DIP
MAX708SESA	-40°C to +85°C	8 SO
MAX708SMJA	-55°C to +125°C	8 CERDIP*
<b>MAX708T</b> CPA	0°C to +70°C	8 Plastic DIP
MAX708TCSA	0°C to +70°C	8 SO
MAX708TCUA	0°C to +70°C	8 $\mu$ MAX
MAX708TEPA	-40°C to +85°C	8 Plastic DIP
MAX708TESA	-40°C to +85°C	8 SO
MAX708TMJA	-55°C to +125°C	8 CERDIP*

\* Contact factory for availability and processing to MIL-STD-883.

# +3V Voltage Monitoring, Low-Cost, $\mu$ P Supervisory Circuits

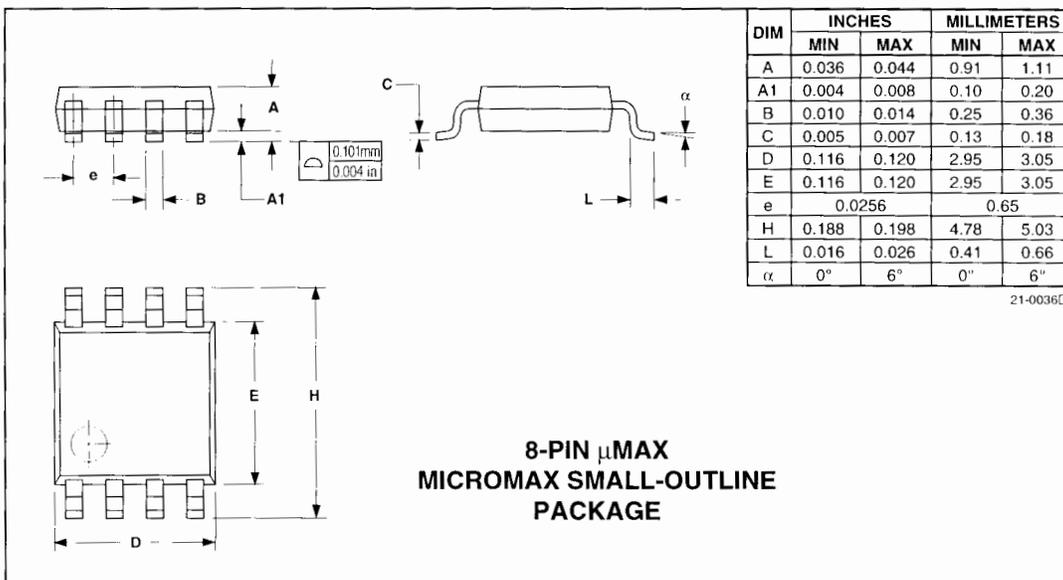
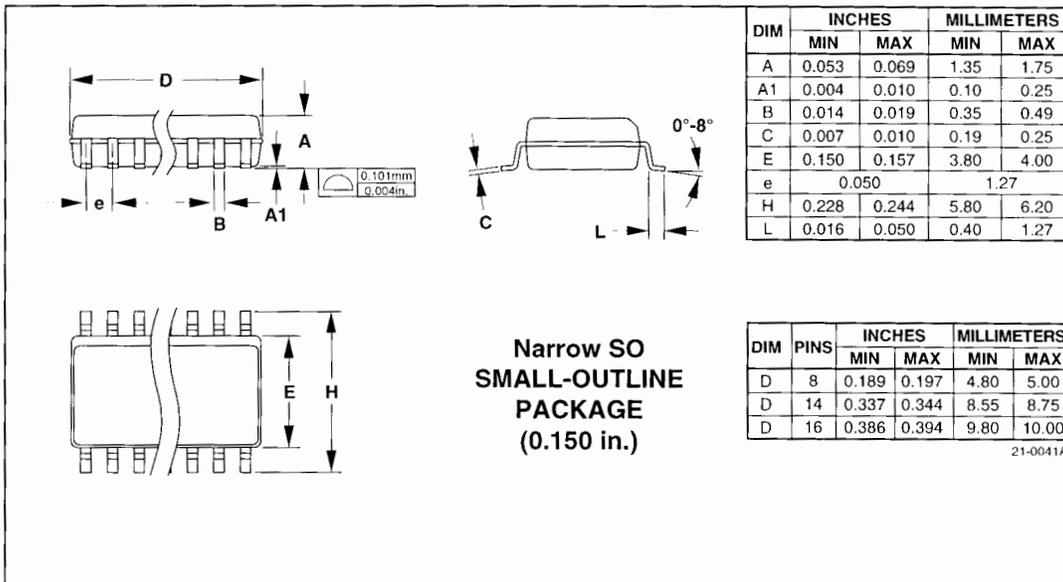
## Package Information

**MAX706P/R/S/T, MAX708R/S/T**



## +3V Voltage Monitoring, Low-Cost, $\mu$ P Supervisory Circuits

### Package Information (continued)



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